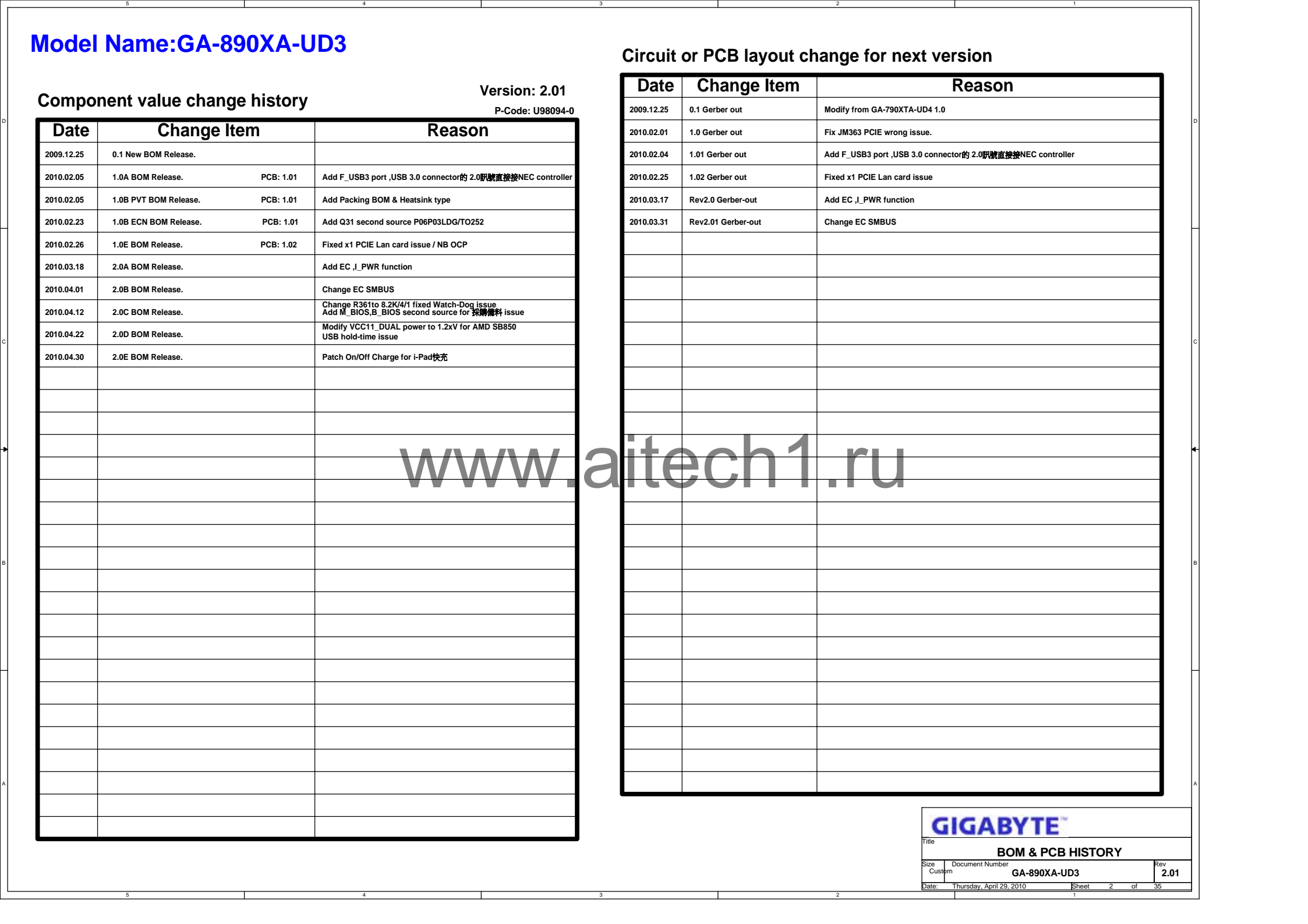
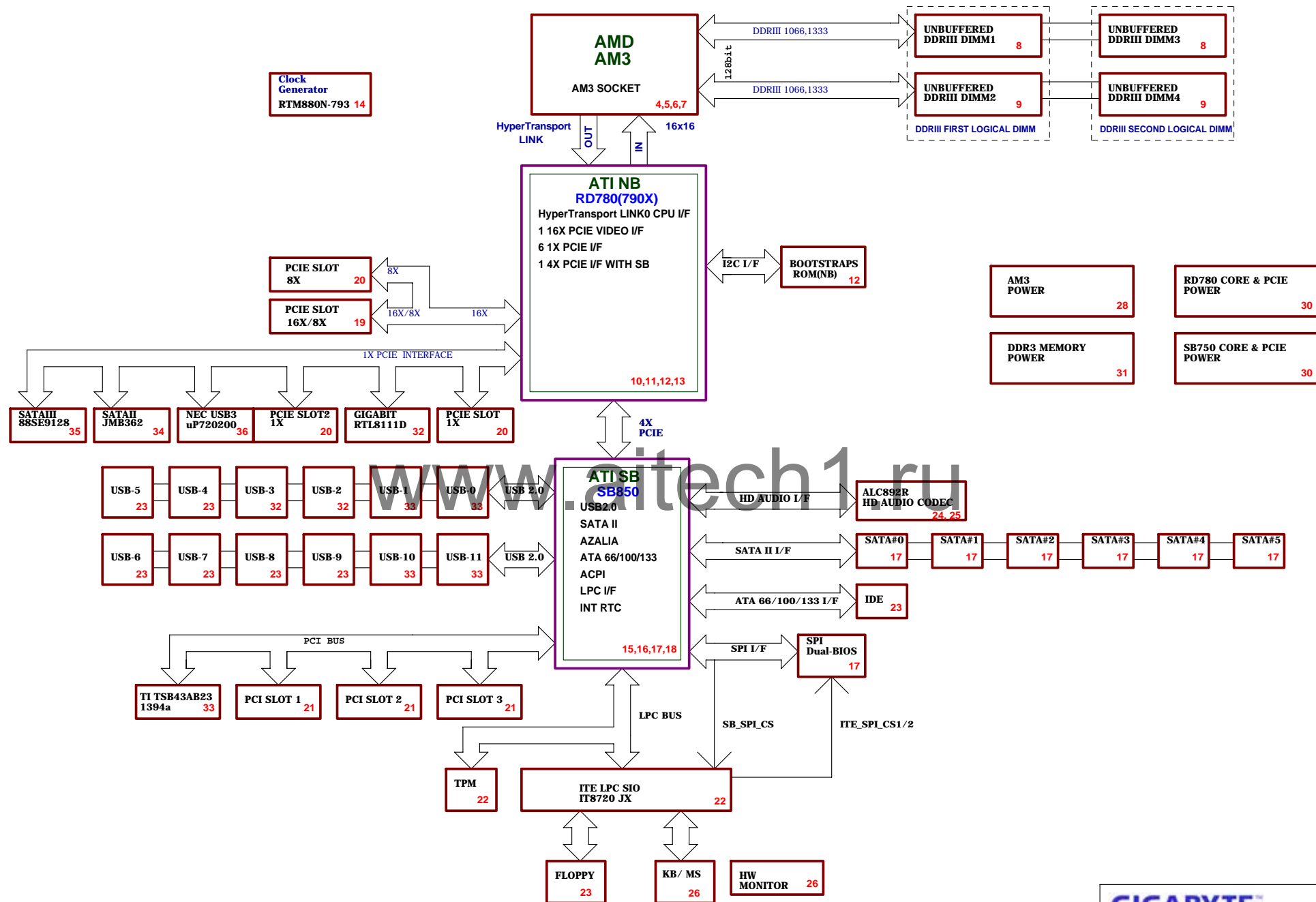


**Revision : 2.01**

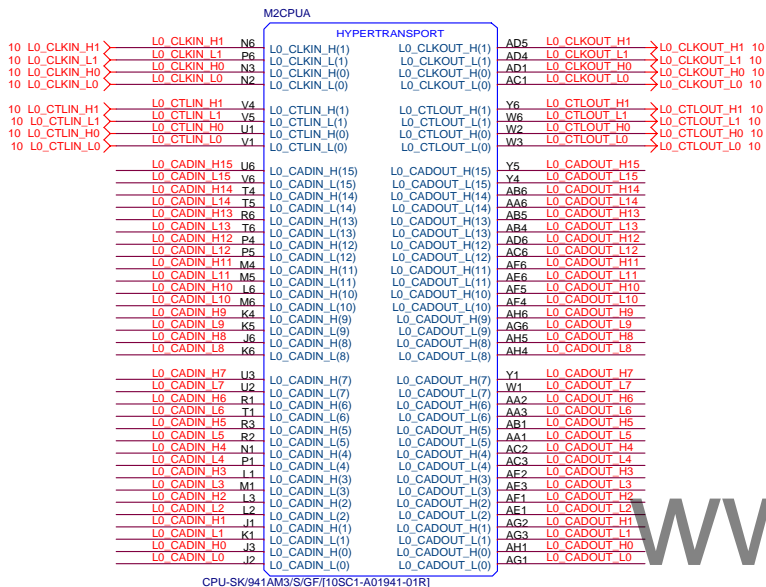
PAGE	TITLE
01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RD780 HT-LINK I/F
11	RD780 PCIE I/F ,SWITCH
12	RD780 SYSTEM I/F
13	RD780 STRAPS ,SPMEM, POWER, GND
14	ICS 9LPR477
15	ATI SB850 PCIE/PCI/CPU/LPC
16	ATI SB850 ACPI/USB/GPIO/AUDIO
17	ATI SB850 SATA/SPI/IDE/HWM
18	ATI SB850 POWER & GND
19	PCI EXPRESS x16
20	PCI_E x8 ,PCI_E x1 SLOT 1,2
21	PCI SLOT 1, 2, 3
22	IT8720 JX LPC IO ,Dual-BIOS ,TPM
23	IDE ,FDD,COM, F_USB, R_USB, I_PWR
24	ALC892R CODEC
25	AUDIO JACK

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L0\_CADIN\_L[0..15] < L0\_CADIN\_L[0..15] 10  
L0\_CADIN\_H[0..15] < L0\_CADIN\_H[0..15] 10  
L0\_CADOUT\_L[0..15] < L0\_CADOUT\_L[0..15] 10  
L0\_CADOUT\_H[0..15] < L0\_CADOUT\_H[0..15] 10



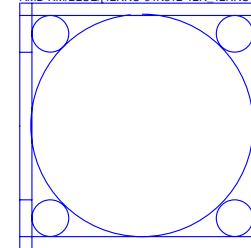
CPU\_VDD\_RUN = VCORE  
CPU\_VDDA\_RUN = VDDA25  
VLDT\_RUN = VCC12\_HT  
CPU\_VDDIO\_SUS = DDR15V  
CPU\_VDDR = CPU\_VDDR12

VLDT\_A = VCC12\_HT  
VLDT\_B = HT12B

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M2CPU  
AMD RM/BLUE/12KRC-04K812-12R\_12KRC-04K812-13R]



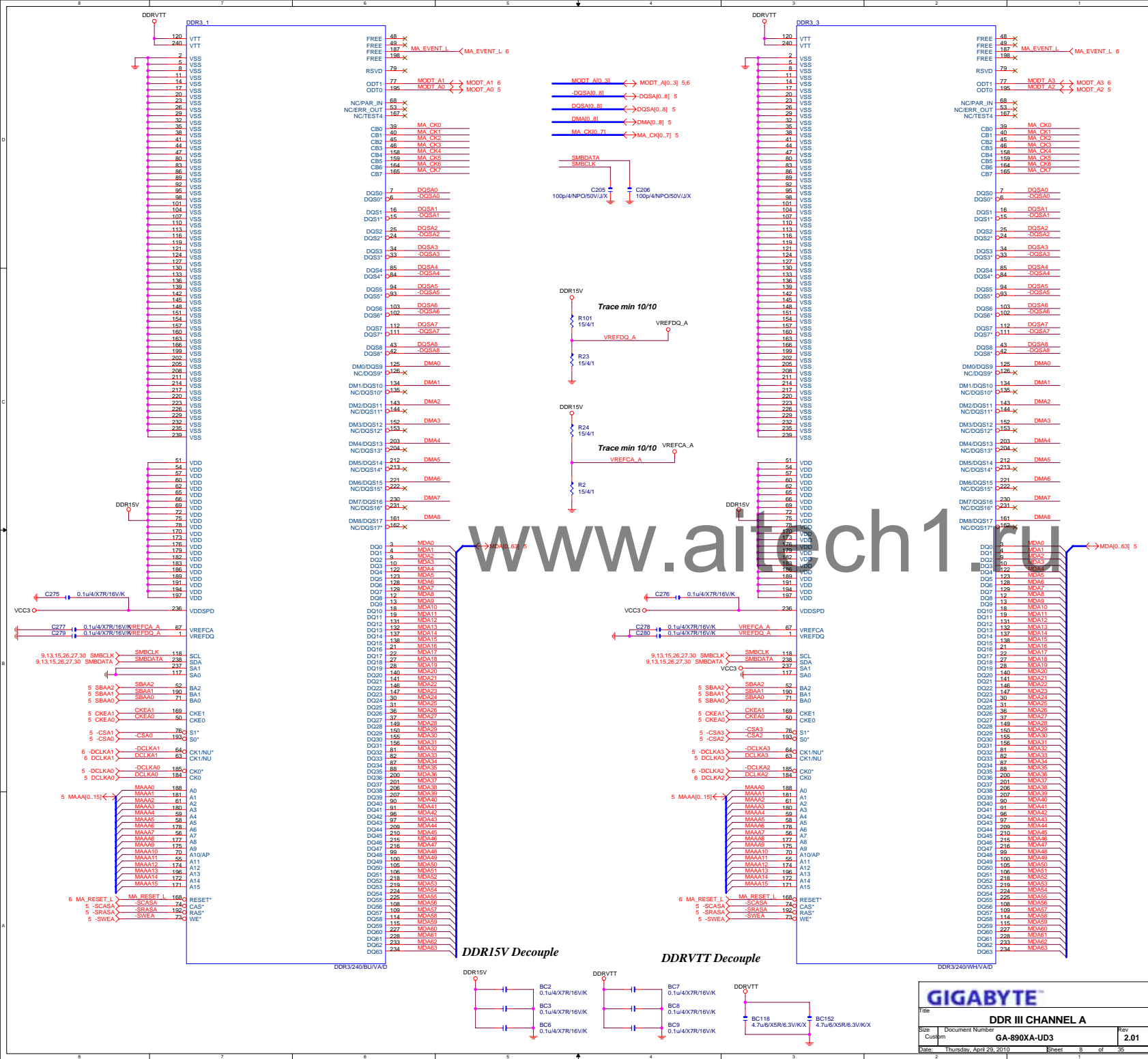
GIGABYTE

Title			
CPU HYPER TRANSPORT			
Size	Document Number	Rev	
Custom	GA-890XA-UD3	2.01	
Date:	Thursday, April 29, 2010	Sheet	4 of 35

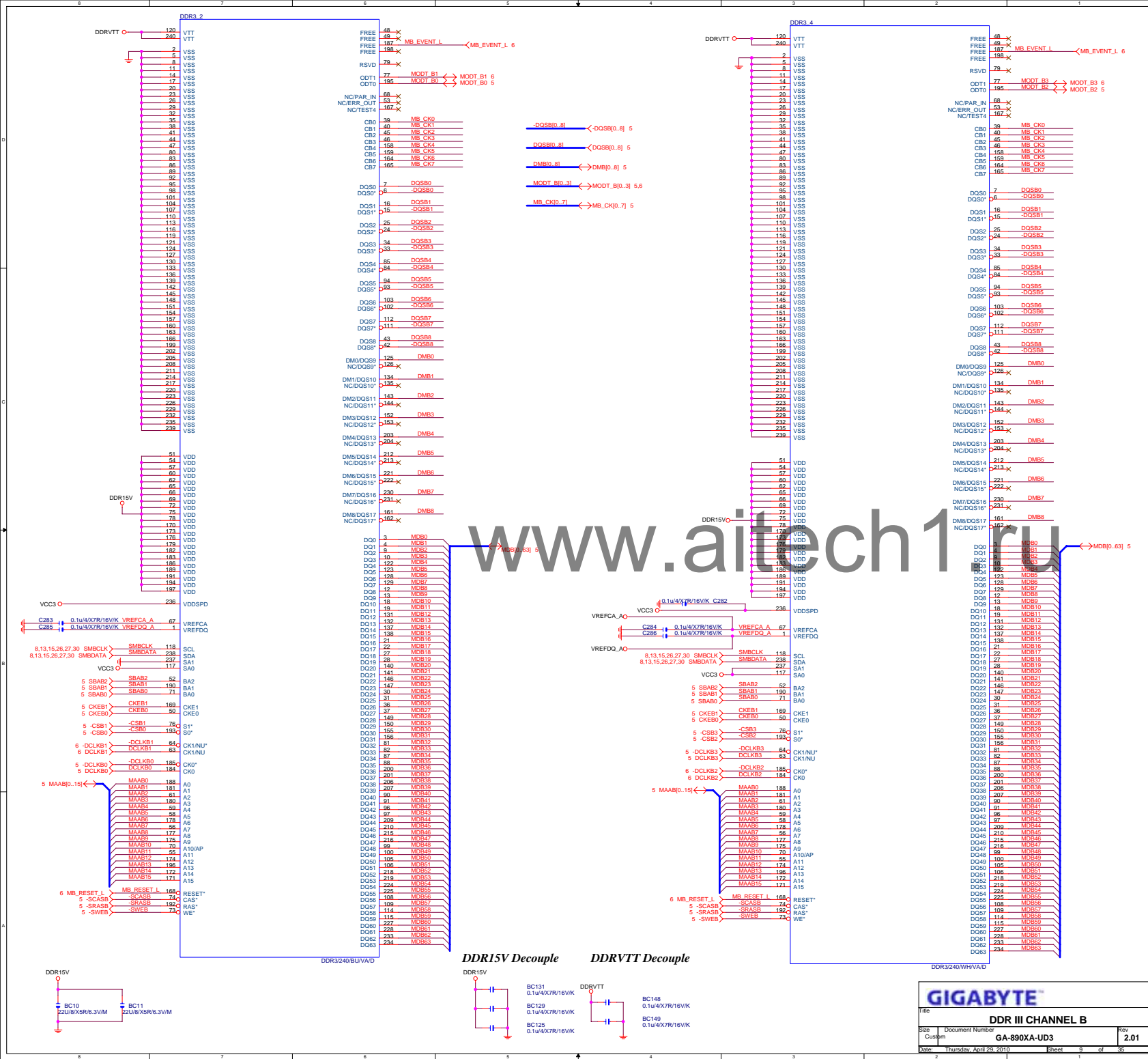


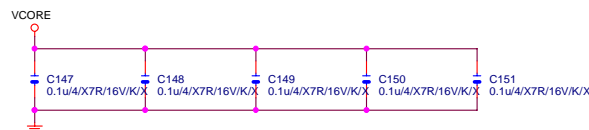
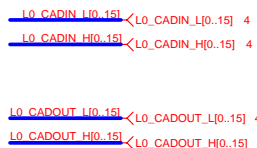




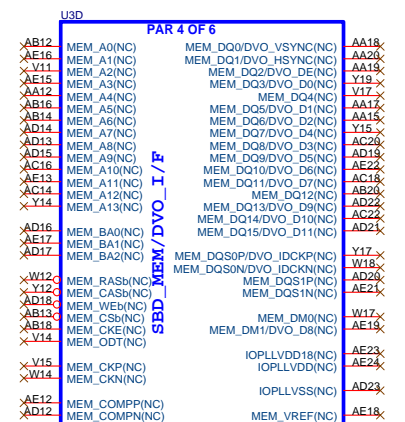
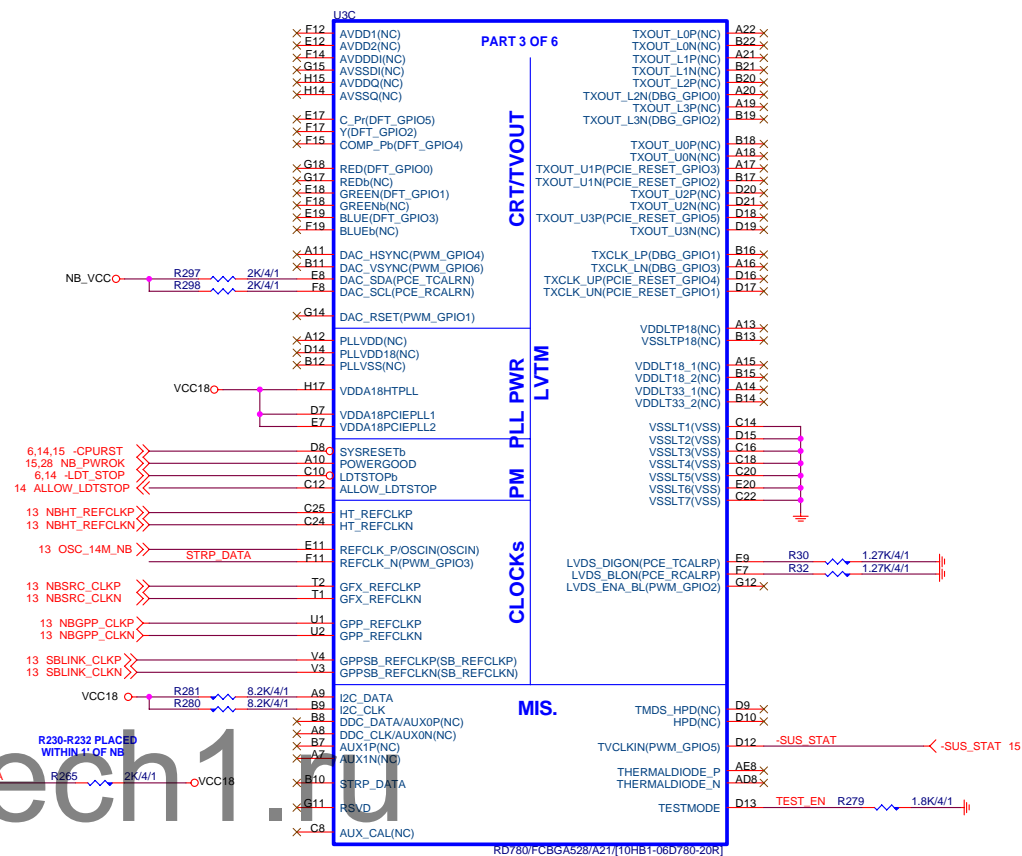
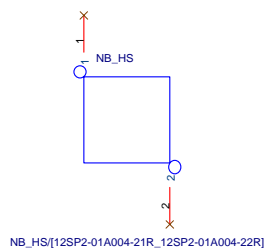




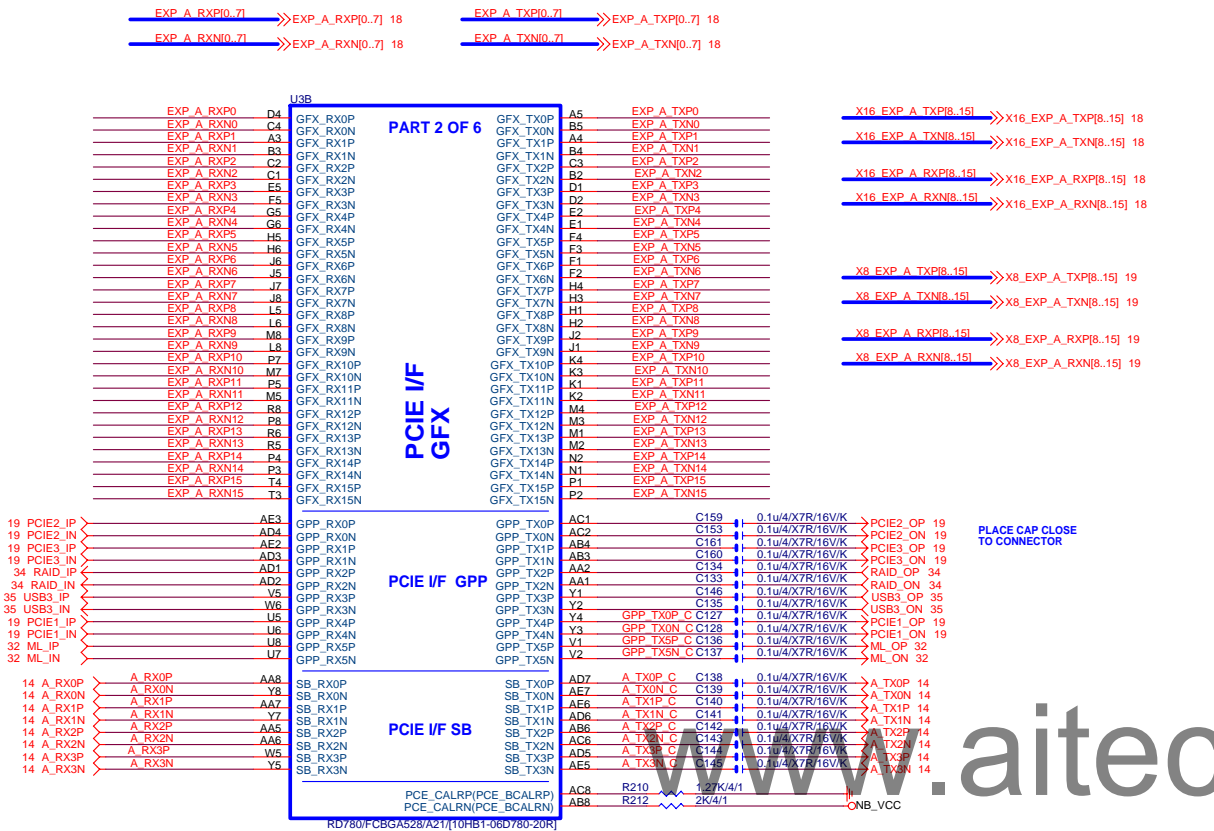




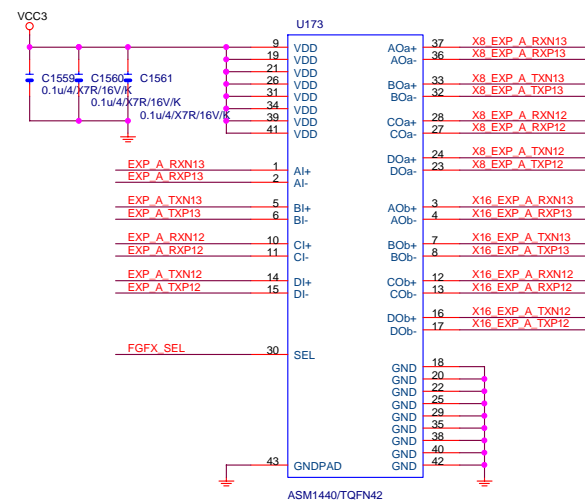
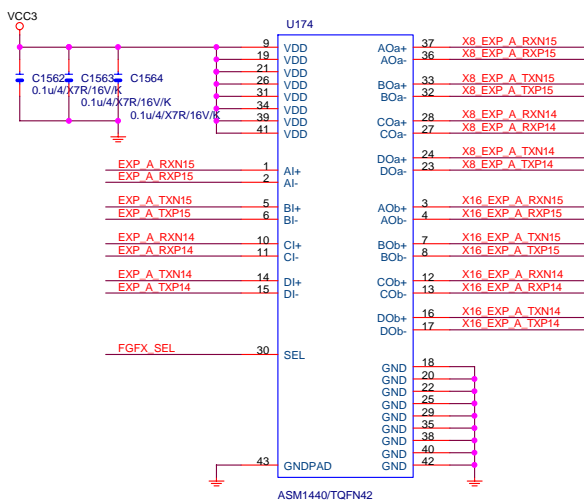
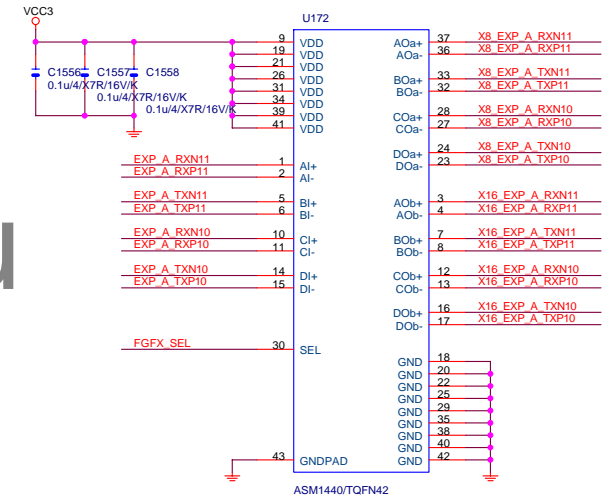
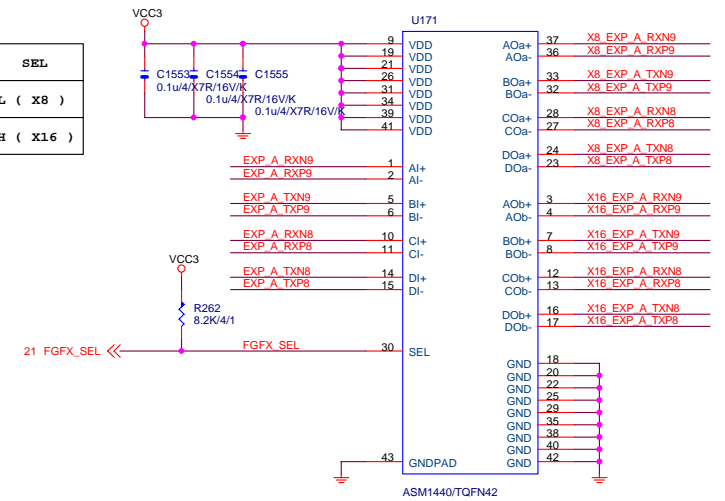
## HT Link Stitching Caps

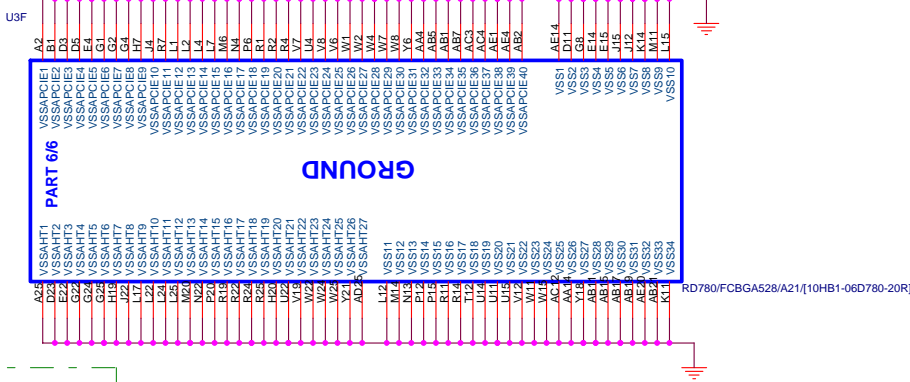


RD780 ALL PIN NC. Aug.15, 2008 confirm--BL

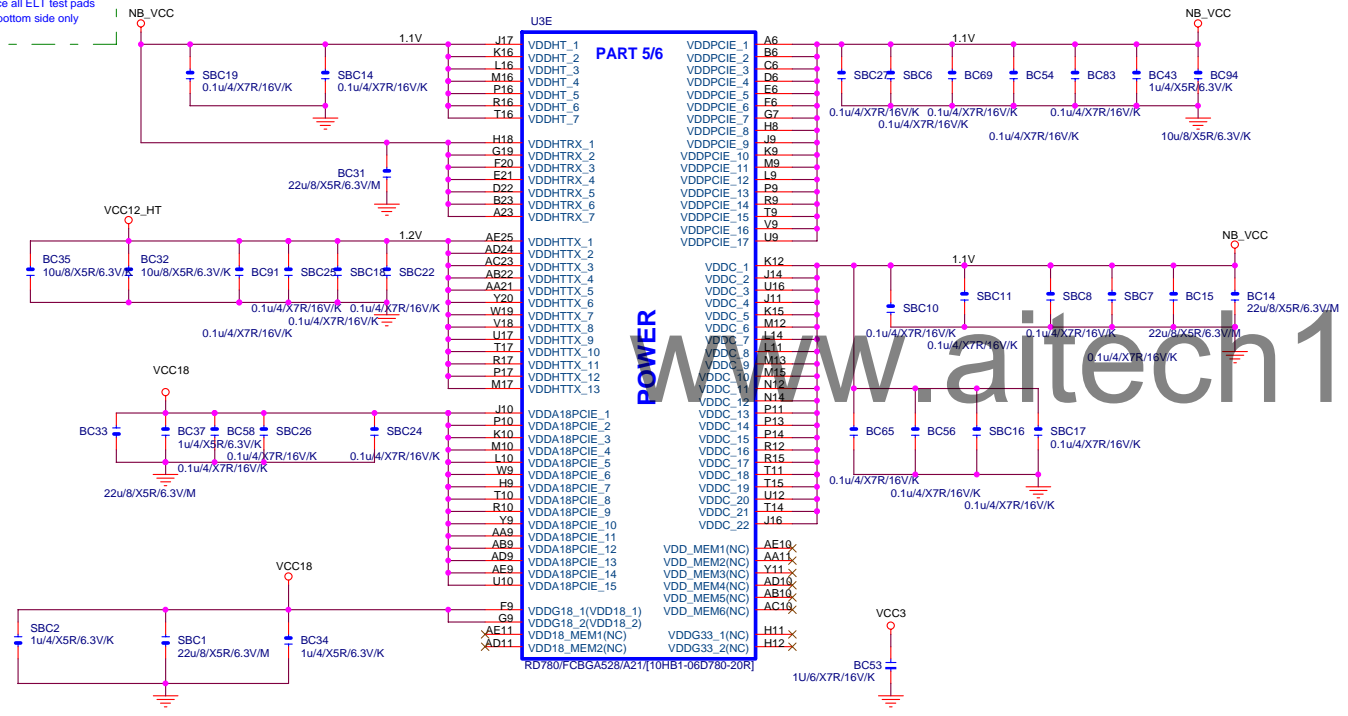


Function	SEL
xI--> xOa	L ( X8 )
xI--> xOb	H ( X16 )





Please use 1mm pad size,  
place all ELT test pads  
on bottom side only



RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC

## RS740/RX780/RS780 STRAPS

### RS740/RX780/RS780: LOAD\_EEPROM\_STRAPS

Selects Loading of STRAPS from EPROM  
1 : Bypass the loading of EEPROM straps and use Hardware Default Values  
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected  
RS740: pin DFT\_GPIO1  
RX780: pin DFT\_GPIO1  
RS780: pin SUS\_STAT#

### RS740/RX780/RS780: STRAP\_DEBUG\_BUS\_GPIO\_ENABLE

Enables the Test Debug Bus using GPIO and/or memory IO  
1 : Disable (RS740/RS780); Enable (RX780)  
0 : Enable (RS740/RS780); Disable(RX780)  
RS740: pin DFT\_GPIO5  
RX780: pin DFT\_GPIO5  
RS780: pin VSYNC

### RS740: STRAP\_PCIE\_SB/GPP\_CFG[2:0] (Pins: RS740\_DFT\_GPIO[4:2])

These pin straps are used to configure PCI-E GPP mode.  
111: register defined (register default to Config E) default  
110: 4-0-0-0-0 Config A  
101: 4-4-0-0-0 Config B  
100: 4-2-2-0-0 Config C  
011: 4-2-1-1-0 Config D  
010: 4-1-1-1-1 Config E  
others: register defined (default to Config E)

### RX780: STRAP\_PCIE\_GPP\_CFG[2:0] (Pins: RX780\_DFT\_GPIO[4:2])

111: 1-1-1-1-1-1 Mode L default  
110: 1-1-1-1-1-1 Mode L  
101: 2-0-2-0-2-0 Mode C2  
100: 2-0-2-0-1-1 Mode K  
011: 2-0-1-1-1-1 Mode E  
010: 1-1-1-1-1-1 Mode L  
001: 4-0-0-0-1-1 Mode C  
000: 4-0-0-0-2-0 Mode B

### RS780: STRAP\_PCIE\_GPP\_CFG[2:0] (configure thru register setting)

1-1-1-1-1-1 Mode L default  
1-1-1-1-1-1 Mode L  
2-0-2-0-2-0 Mode C2  
2-0-2-0-1-1 Mode K  
2-0-1-1-1-1 Mode E  
1-1-1-1-1-1 Mode L  
4-0-0-0-1-1 Mode C  
4-0-0-0-2-0 Mode B

### RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

Enables Side port memory  
1. Disable (RS740/RS780)  
0 : Enable (RS740/RS780)  
RS740: pin DFT\_GPIO0  
RS780: pin HSYNC  
RX780: Not Applicable

### RX780/RS780: STRAP\_DEBUG\_BUS\_PCIE\_ENABLE

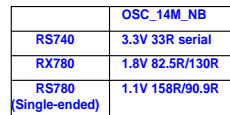
Enables Test debug bus using PCIE bus  
1. Disable (can be enabled thru nbcfg register)  
0 : Enable  
RX780: pin DFT\_GPIO0  
RS780: configurable thru register setting only  
RS740: Not supported



- Place R800/801 less than 500 mils away from U800  
R851 less than 100 mils away from R800/801  
route CPU clock as 100ohm differential pair

NB CLOCKS		RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF		
HT_REFCLKN	NC	100M DIFF	100M DIFF		
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF	
REFCLK_N	NC	NC	vref	100M DIFF	
GF_X_REFCLK*	100M DIFF	100M DIFF	100M DIFF		
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)		
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF		

\* the GFX\_REFCLK input is required for all cases



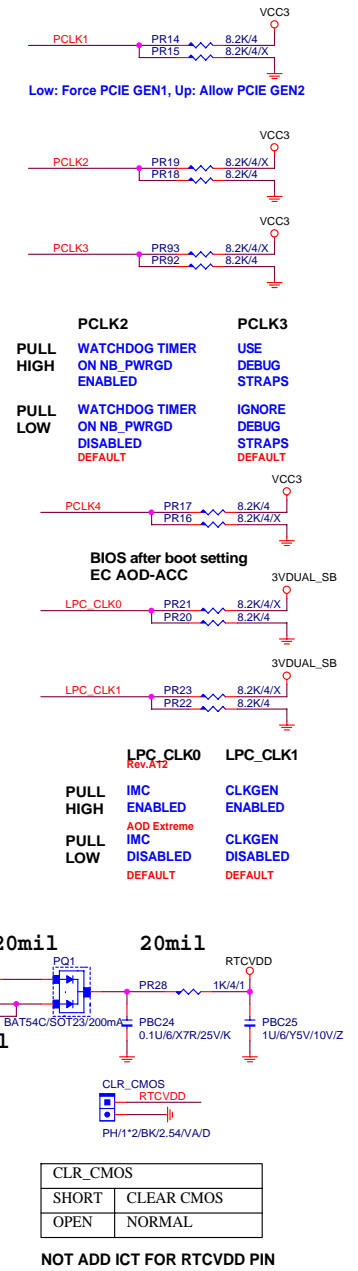
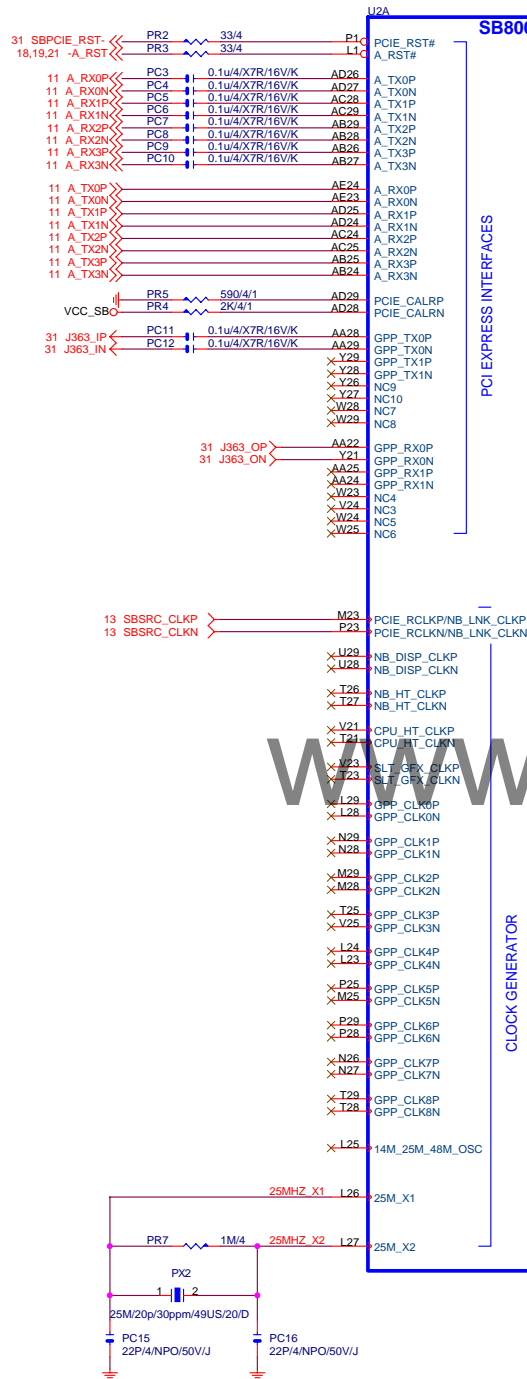
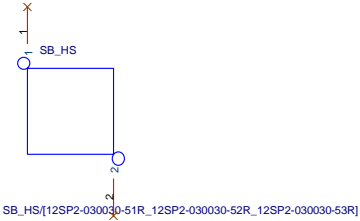
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

# S.B HEATSINK



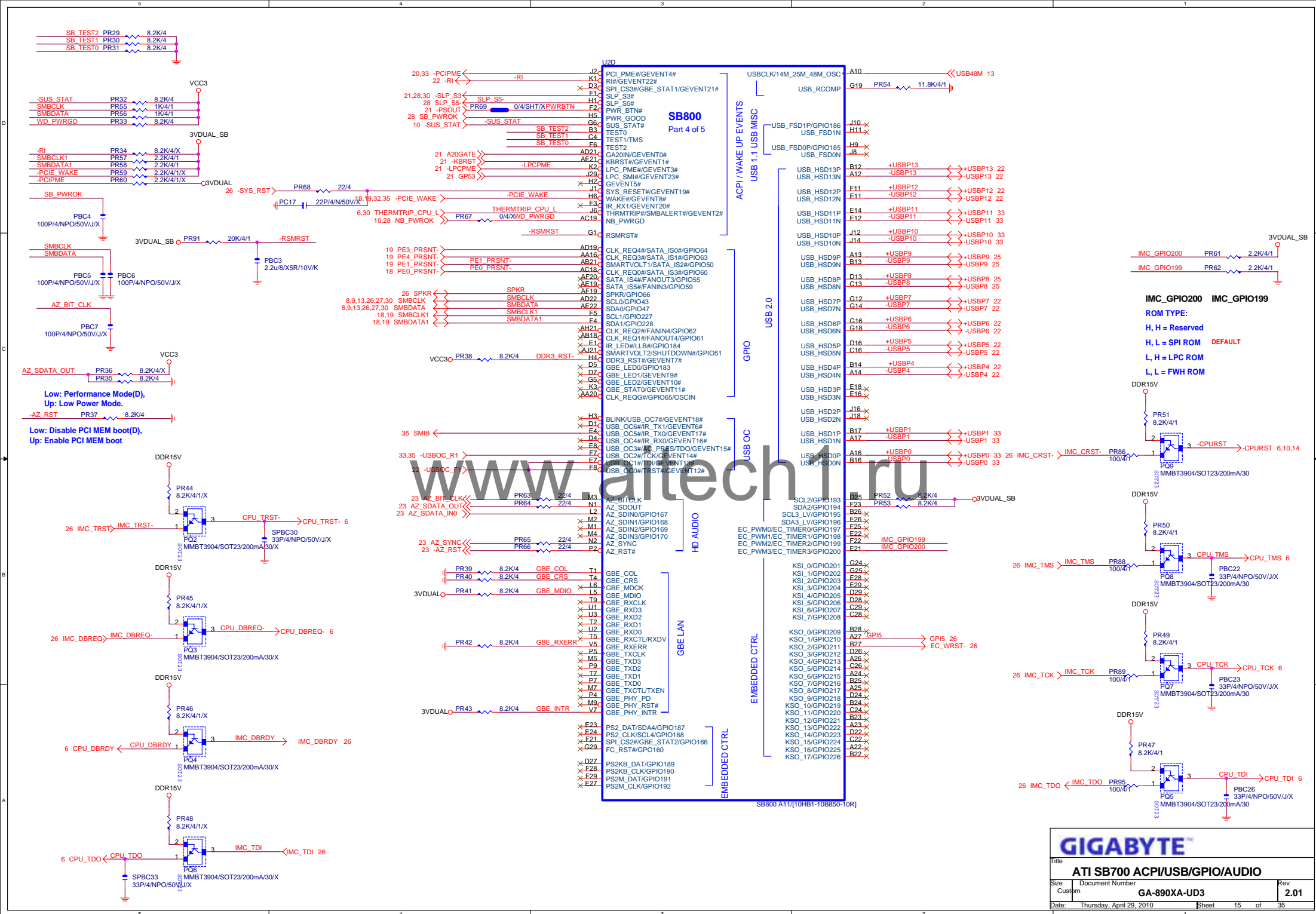
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850



**GIGABYTE**

Title			ATI SB700 PCI/PCI/CPU/LPC
Size	Document Number	Rev	2.01
Custom	GA-890XA-UD3		
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PLACE SATA CAL  
RES VERY CLOSE  
TO BALL OF U600

**NOTE:**

R650 IS 1K 1% FOR 25MHz  
XTAL, 4.99K 1% FOR 100MHz  
INTERNAL CLOCK

SP\_TX0P\_C AH9  
SP\_TX0M\_C AJ9  
SP\_RX0M\_C AJ8  
SP\_RX0P\_C AH8  
SP\_TX1P\_C AH10  
SP\_TX1M\_C AJ10  
SP\_RX1M\_C AG10  
SP\_RX1P\_C AF10  
SP\_TX2P\_C AG12  
SP\_TX2M\_C AF12  
SP\_RX2M\_C AJ12  
SP\_RX2P\_C AH12  
SP\_TX3P\_C AH14  
SP\_TX3M\_C AJ14  
SP\_RX3M\_C AG14  
SP\_RX3P\_C AF14  
SP\_TX4P\_C AG17  
SP\_TX4M\_C AF17  
SP\_RX4M\_C AJ17  
SP\_RX4P\_C AH17  
SP\_TX5P\_C AJ18  
SP\_TX5M\_C AH18  
SP\_RX5M\_C AH19  
SP\_RX5P\_C AJ19

U2B

**SB800**  
Part 2 of 5

GPIOD

SERIAL ATA

HW MONITOR

SPI FROM

FC\_CLK AH28  
FC\_FBCLKOUT AG28  
FC\_FBCLKIN AF28  
FC\_OE#/GPIOD145 AF28  
FC\_AVD#/GPIOD146 AG28  
FC\_VWE#/GPIOD148 AG28  
FC\_CE1#/GPIOD149 AF28  
FC\_CE2#/GPIOD150 AE28  
FC\_INT1#/GPIOD144 AF28  
FC\_INT2#/GPIOD147 AH28  
FC\_ADQ0#/GPIOD128 AJ27  
FC\_ADQ1#/GPIOD129 AJ26  
FC\_ADQ2#/GPIOD130 AH25  
FC\_ADQ3#/GPIOD131 AH24  
FC\_ADQ4#/GPIOD132 AG24  
FC\_ADQ5#/GPIOD133 AH23  
FC\_ADQ6#/GPIOD134 AG23  
FC\_ADQ7#/GPIOD135 AF21  
FC\_ADQ8#/GPIOD136 AF22  
FC\_ADQ9#/GPIOD137 AH22  
FC\_ADQ10#/GPIOD138 AJ25  
FC\_ADQ11#/GPIOD139 AJ24  
FC\_ADQ12#/GPIOD140 AJ25  
FC\_ADQ13#/GPIOD141 AJ25  
FC\_ADQ14#/GPIOD142 AG25  
FC\_ADQ15#/GPIOD143 AH25

FANOUT0/GPIO52 W5  
FANOUT1/GPIO53 Y9  
FANOUT2/GPIO54 Y9  
FANIN0/GPIO56 W7  
FANIN1/GPIO57 Y9  
FANIN2/GPIO58 W8

TEMPIN0/GPIO171 B6  
TEMPIN1/GPIO172 A6  
TEMPIN2/GPIO173 A5  
TEMPIN3/TALERT#/GPIO174 B5  
TEMP\_COMM C7

VIN0/GPIO175 A3  
VIN1/GPIO176 B4  
VIN2/GPIO177 A4  
VIN3/GPIO178 C5  
VIN4/GPIO179 A7  
VIN5/GPIO180 B7  
VIN6/GBE\_STAT3/GPIO181 B8  
VIN7/GBE\_LED3/GPIO182 A8

NC1 G27  
NC2 G28

VCC\_SBC PR75 1K/4/1 SATA\_CALRP AB14  
PR74 931/4/1 SATA\_CALRN AA14

SATA\_X2 26 -SATA\_LED -SATA\_LED AD11

SATA\_X1 AD16

SATA\_X2 AC16

PC42 22P/4/NPO/50V/J/X

PC43 22P/4/NPO/50V/J/X

SB\_SPI\_DI PR70 22/4 SB\_SPI\_DI\_R J5

SB\_SPI\_DO PR71 22/4 SB\_SPI\_DO\_R E2

SB\_SPI\_CLK PR72 22/4 SB\_SPI\_CLK\_R K4

SB\_SPI\_CS\_ITE PR73 22/4 SB\_SPI\_CS\_ K9

SB\_SPI\_CS\_ITE PR73 22/4 SB\_SPI\_CS\_ K9

SB\_SPI\_CS\_ITE PR73 22/4 SB\_SPI\_CS\_ K9

SB\_SPI\_CS\_ITE PR73 22/4 SB\_SPI\_CS\_ K9

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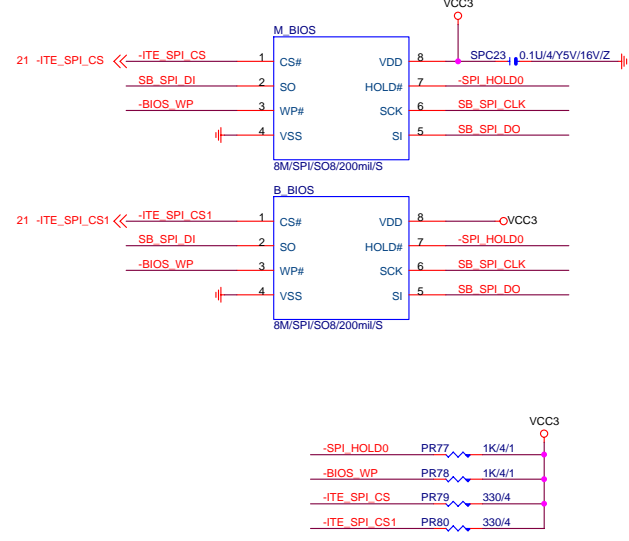
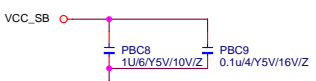
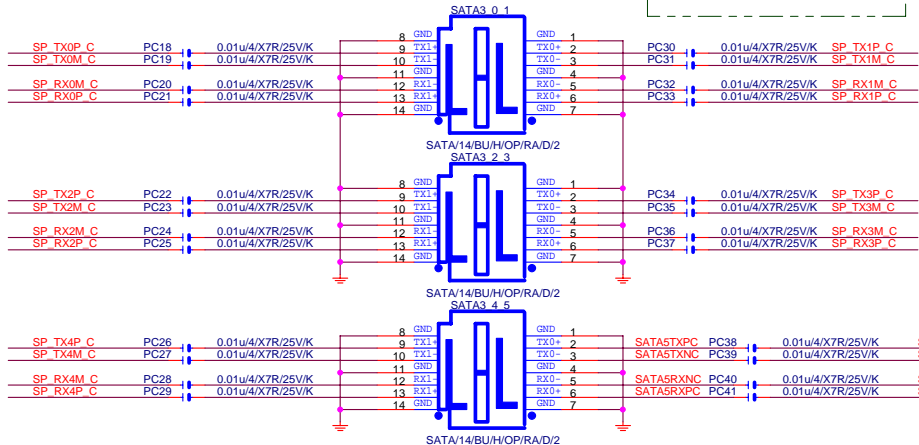
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SB\_SPI\_CS\_ITE PR73 22/4 SB\_SPI\_CS\_ K9

SB\_SPI\_CS\_ITE PR73 22/4 SB\_SPI\_CS\_ K9



PLACE SATA AC COUPLING  
CAPS CLOSE TO SB850

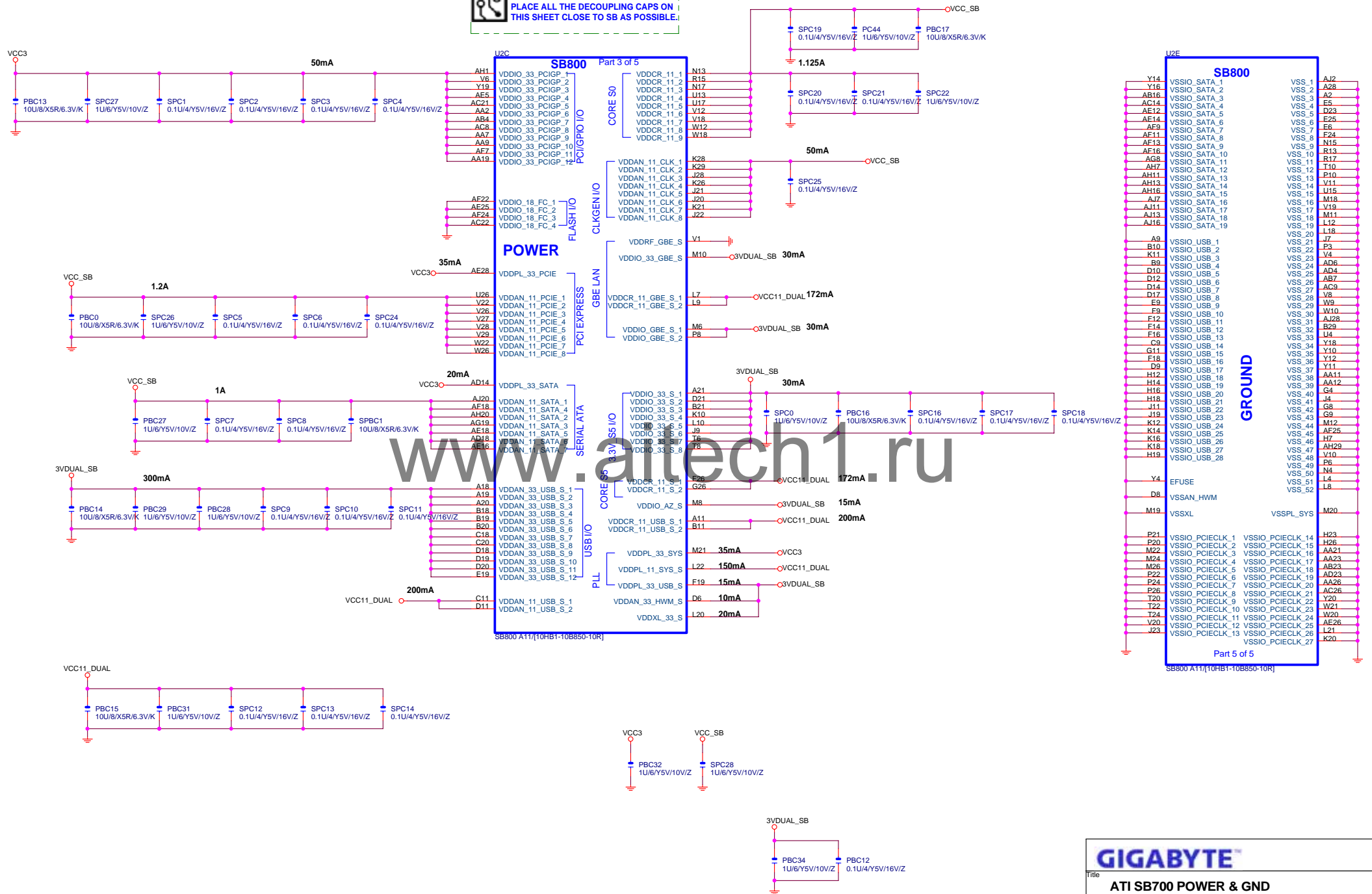


GIGABYTE		
Title		
ATI SB700 SATA/IDE/HWM/SPI		
Size	Document Number	Rev
Custm	GA-890XA-UD3	2.01
Date:	Thursday, April 29, 2010	Sheet 16 of 35

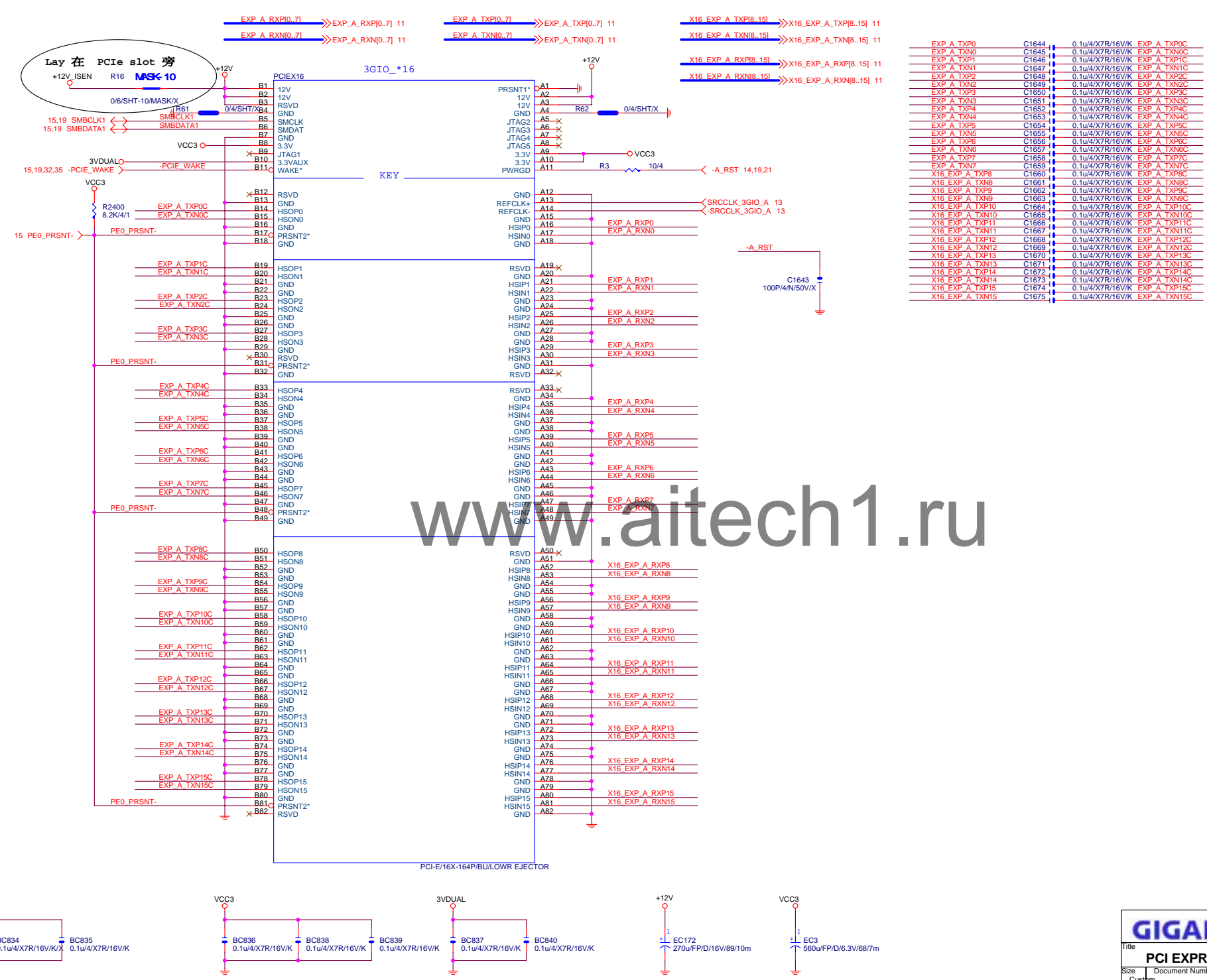




PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



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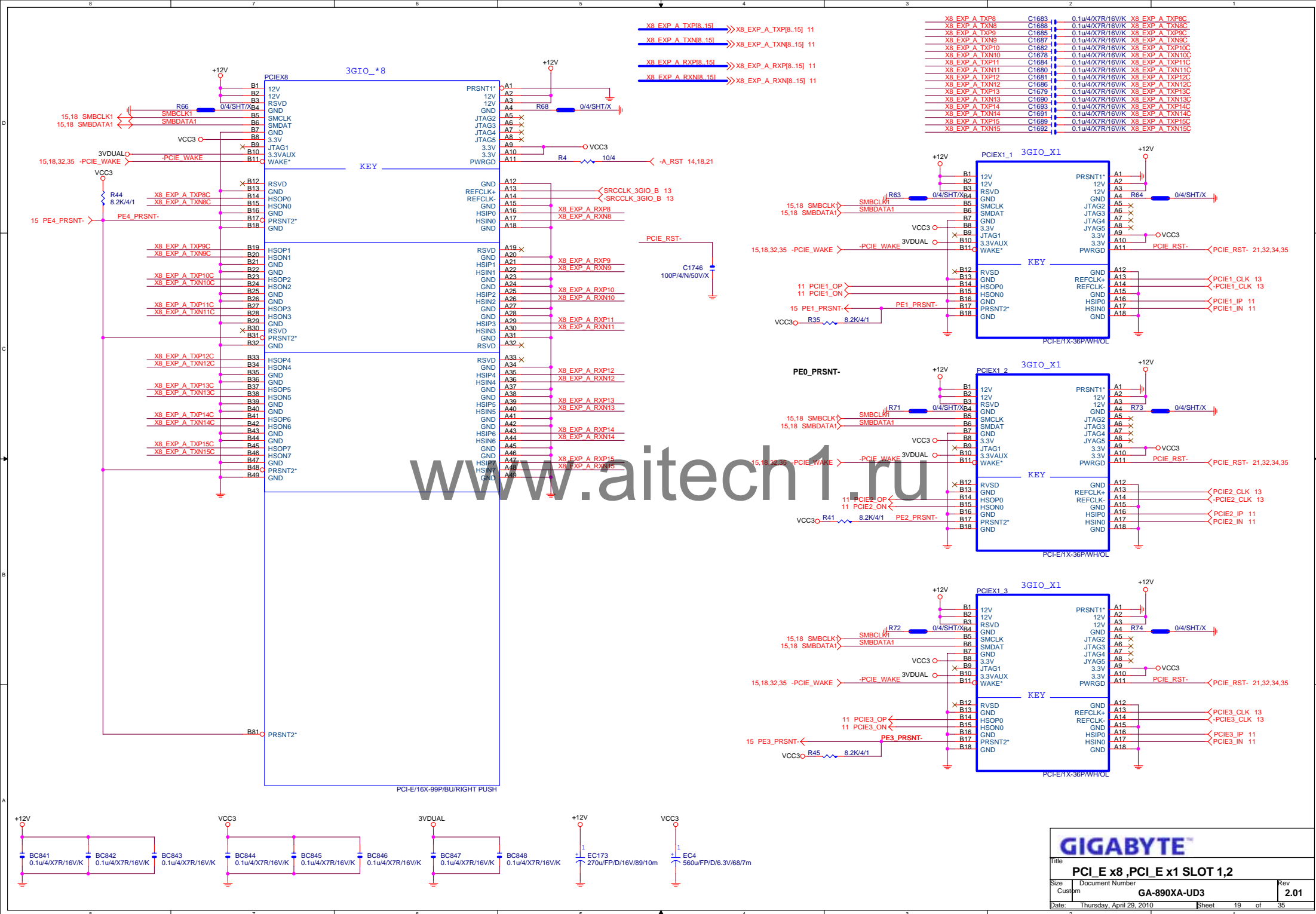
**GIGABYTE**

PCI EXPRESS X 16 ,X1

Document Number  
GA-890XA-UD3

Rev  
2.01

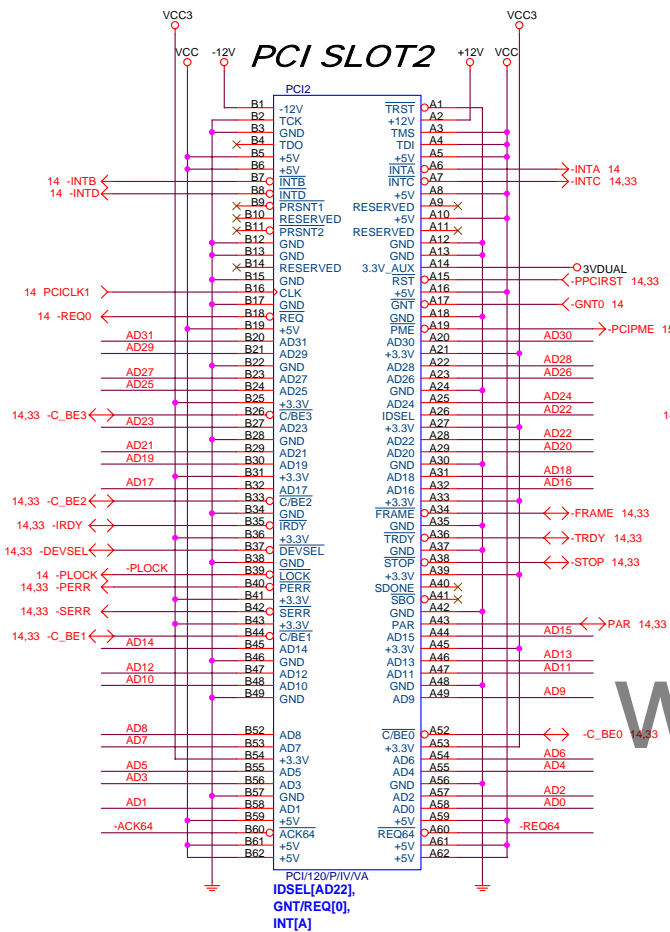
Date: Thursday, April 29, 2010 Sheet 18 of 35



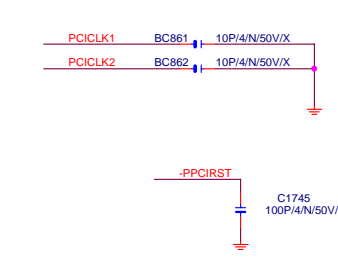
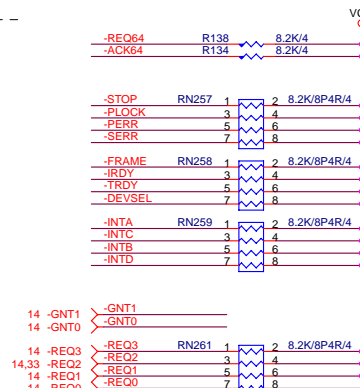
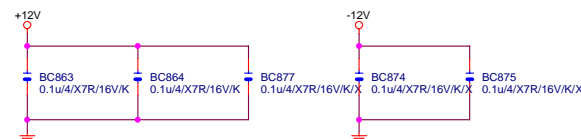
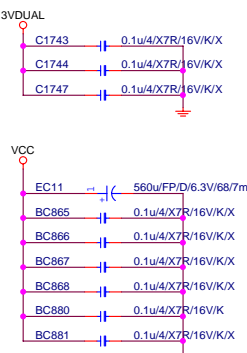
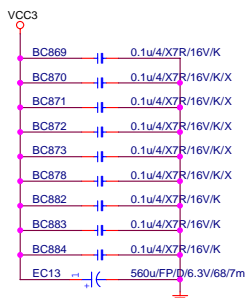
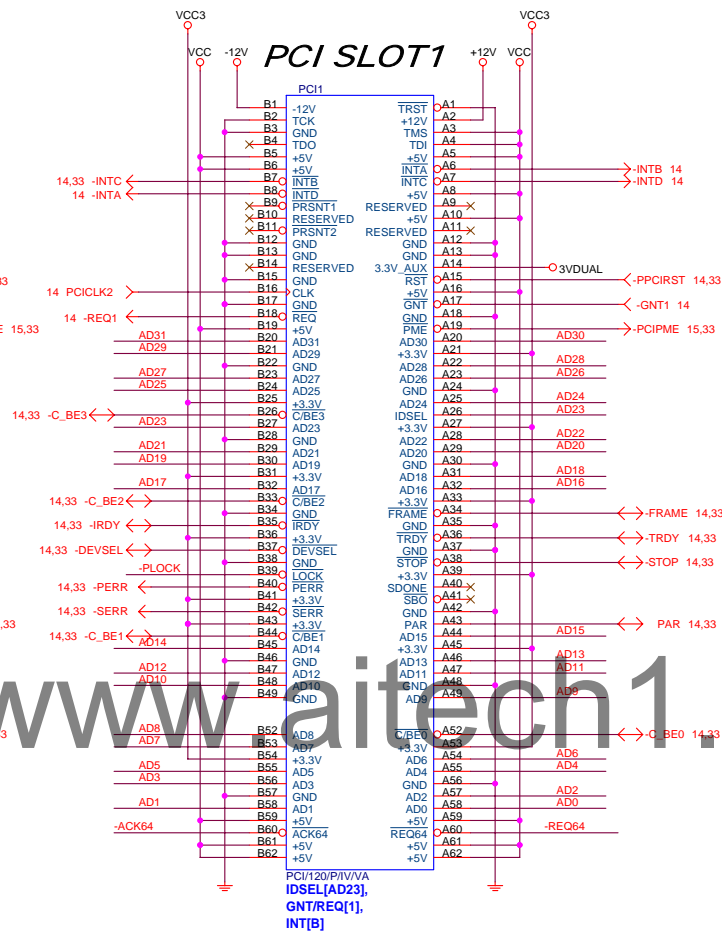
# PCI SLOT 1,2

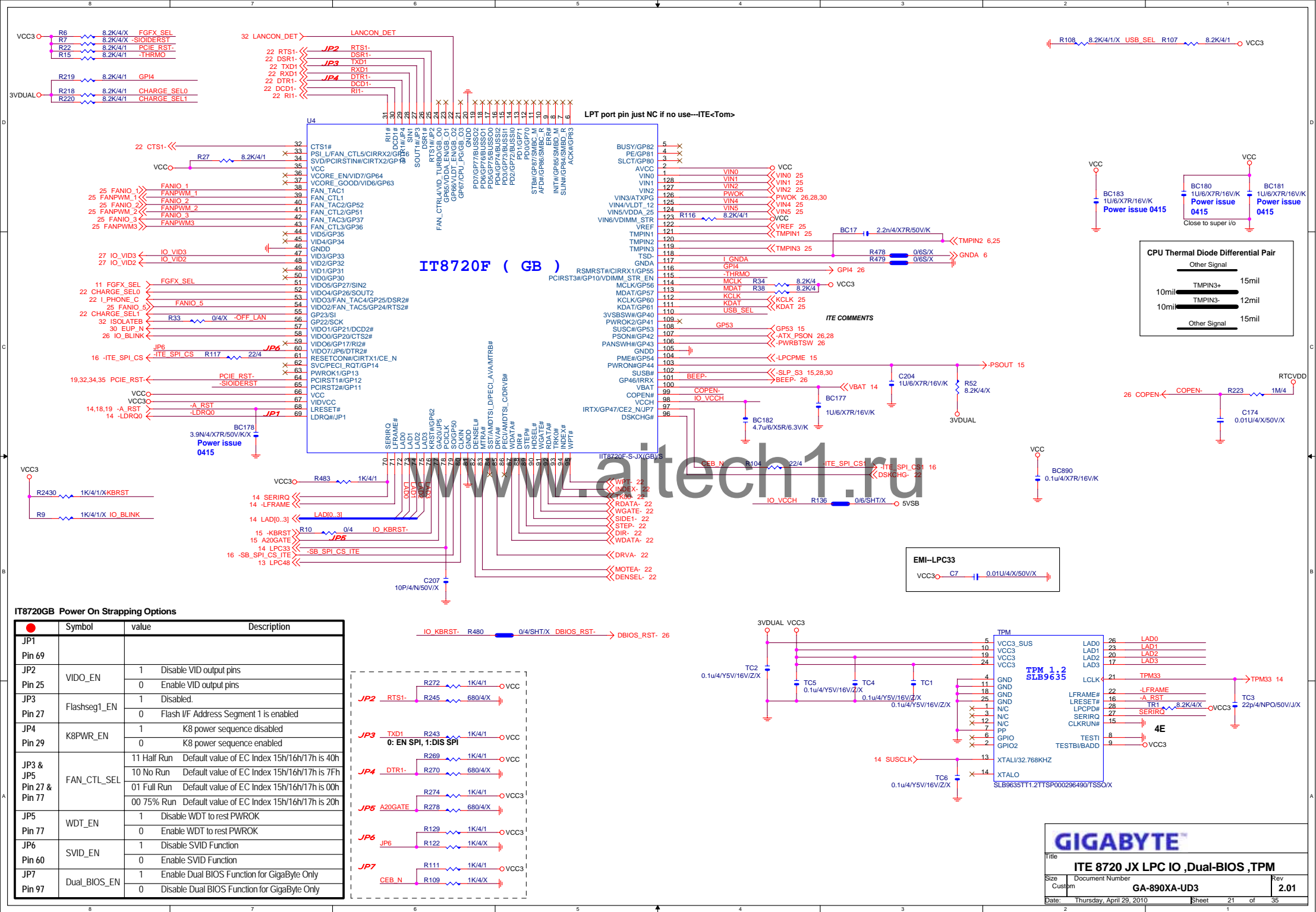
14,33 AD[0..31] ↔ AD[0..31]

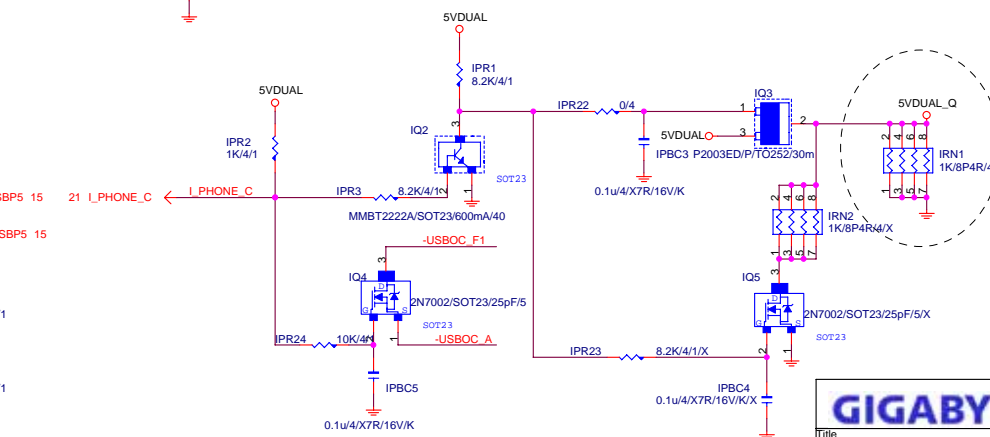
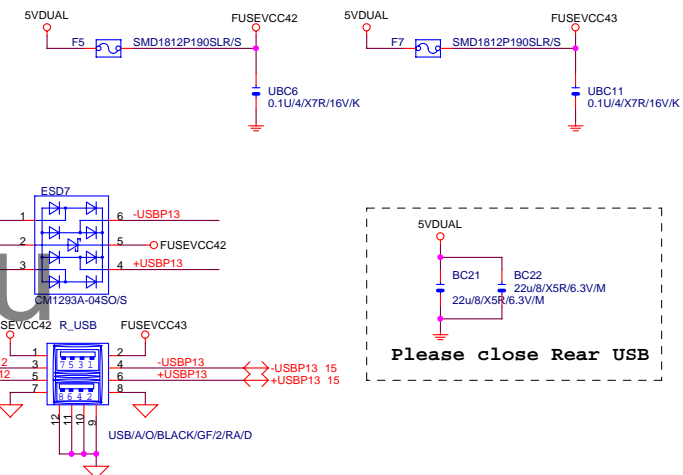
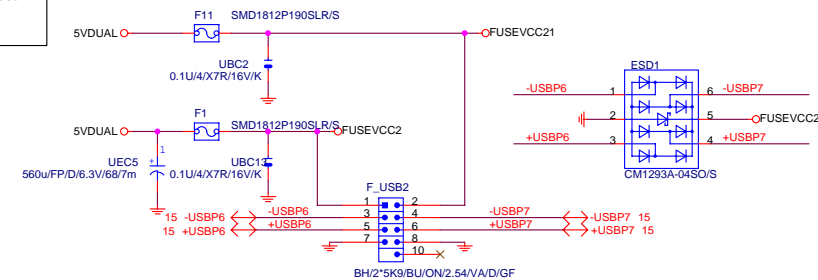
## PCI SLOT2



## PCI SLOT1





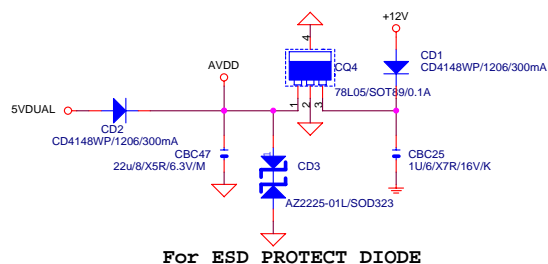
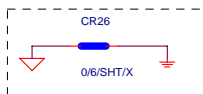


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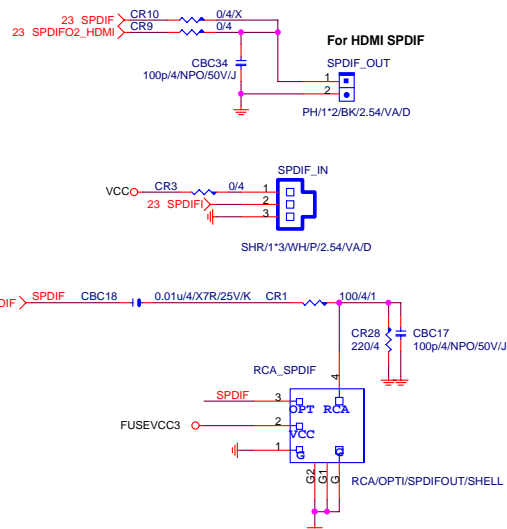
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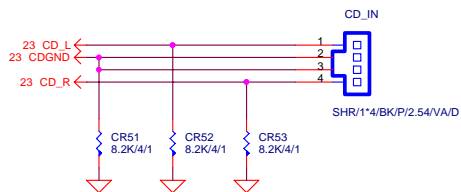
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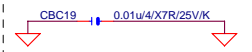
## SPDIF



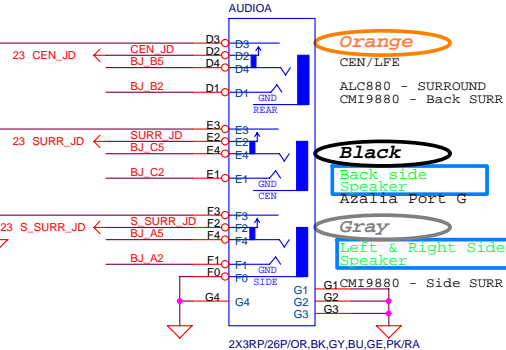
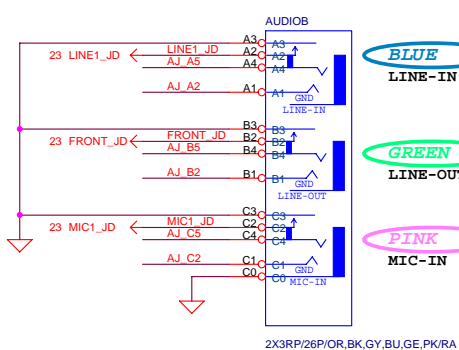
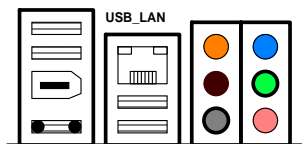
## CD IN



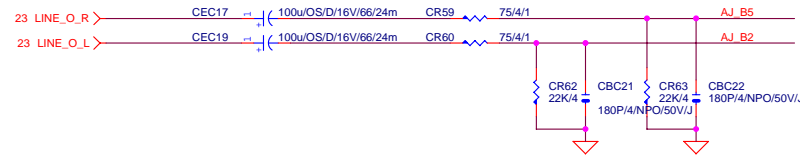
## For Audio precision test



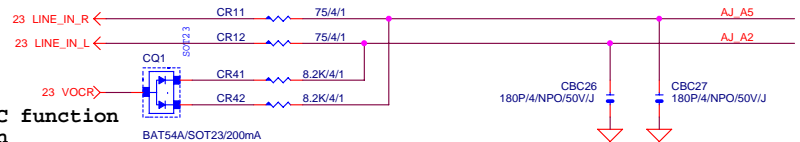
## USB\_1394\_ESATA



## LINE OUT FRONT OUT

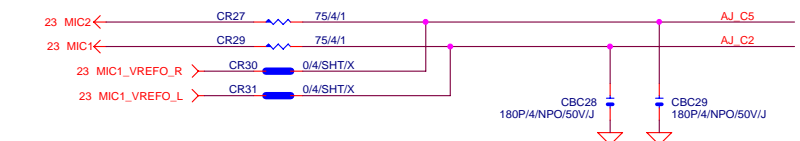


## LINE-IN

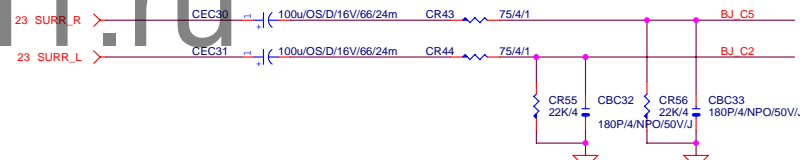


Verify MIC function in LINE-in

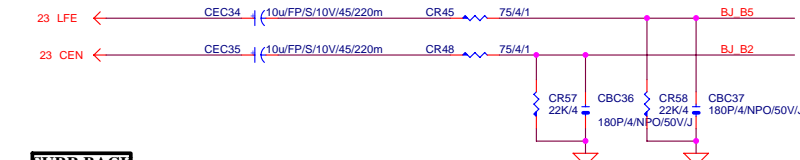
## MIC



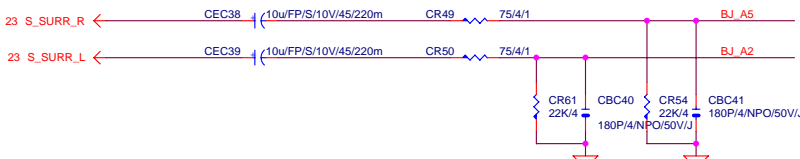
## SURROUND



## CEN/LFE



## SURR BACK



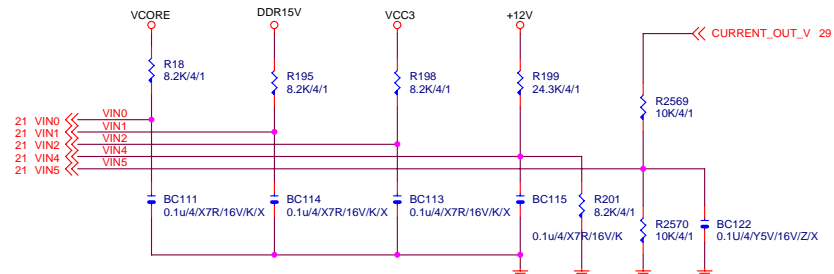
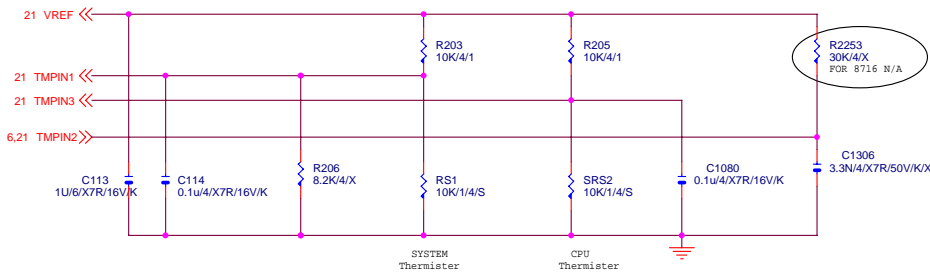
**GIGABYTE**

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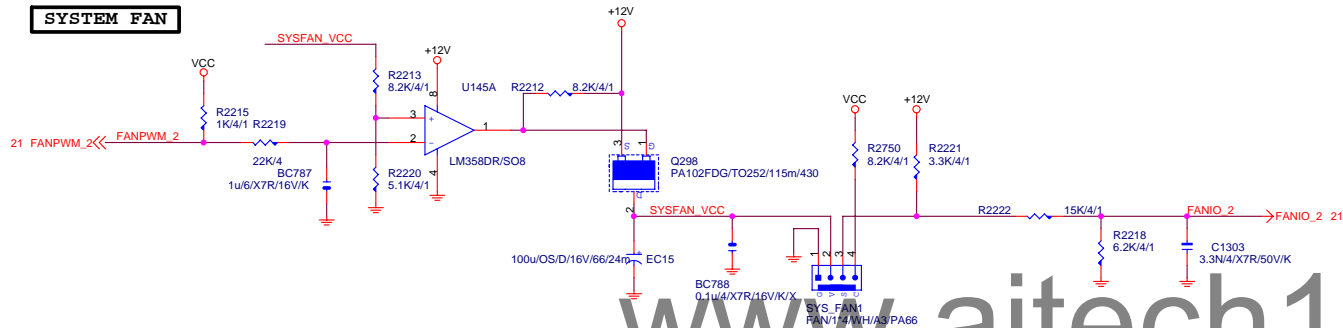
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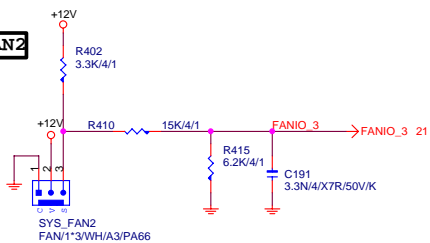
## Hardware Monitor circuits



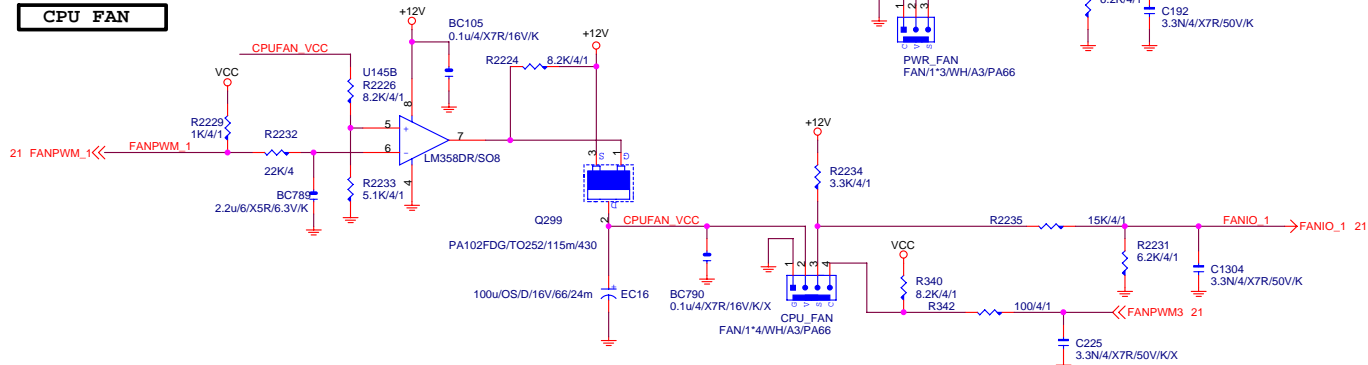
## SYSTEM FAN



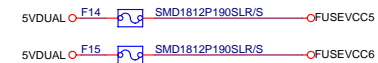
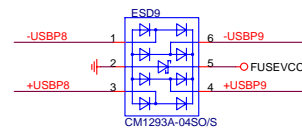
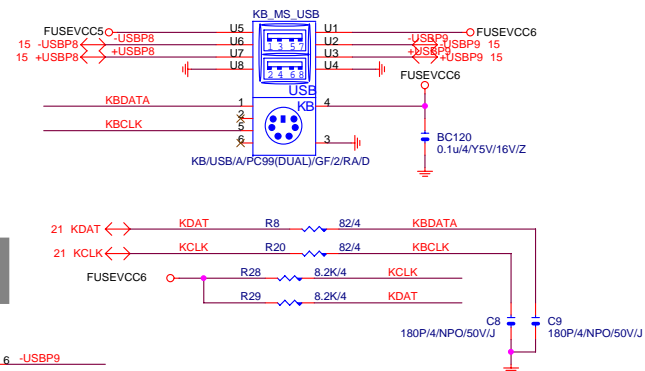
## SYSTEM FAN2



## CPU FAN

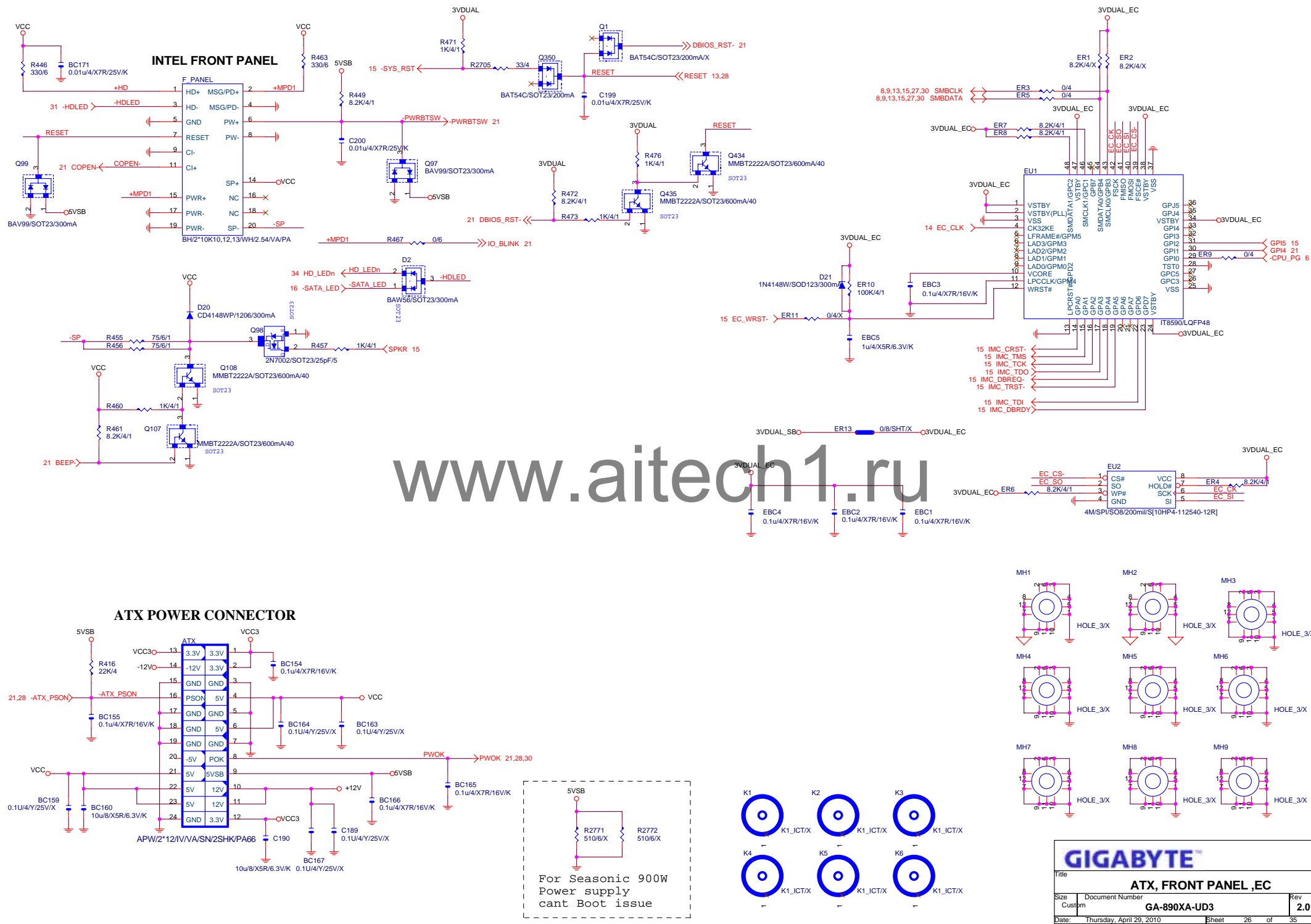


## KB & USB



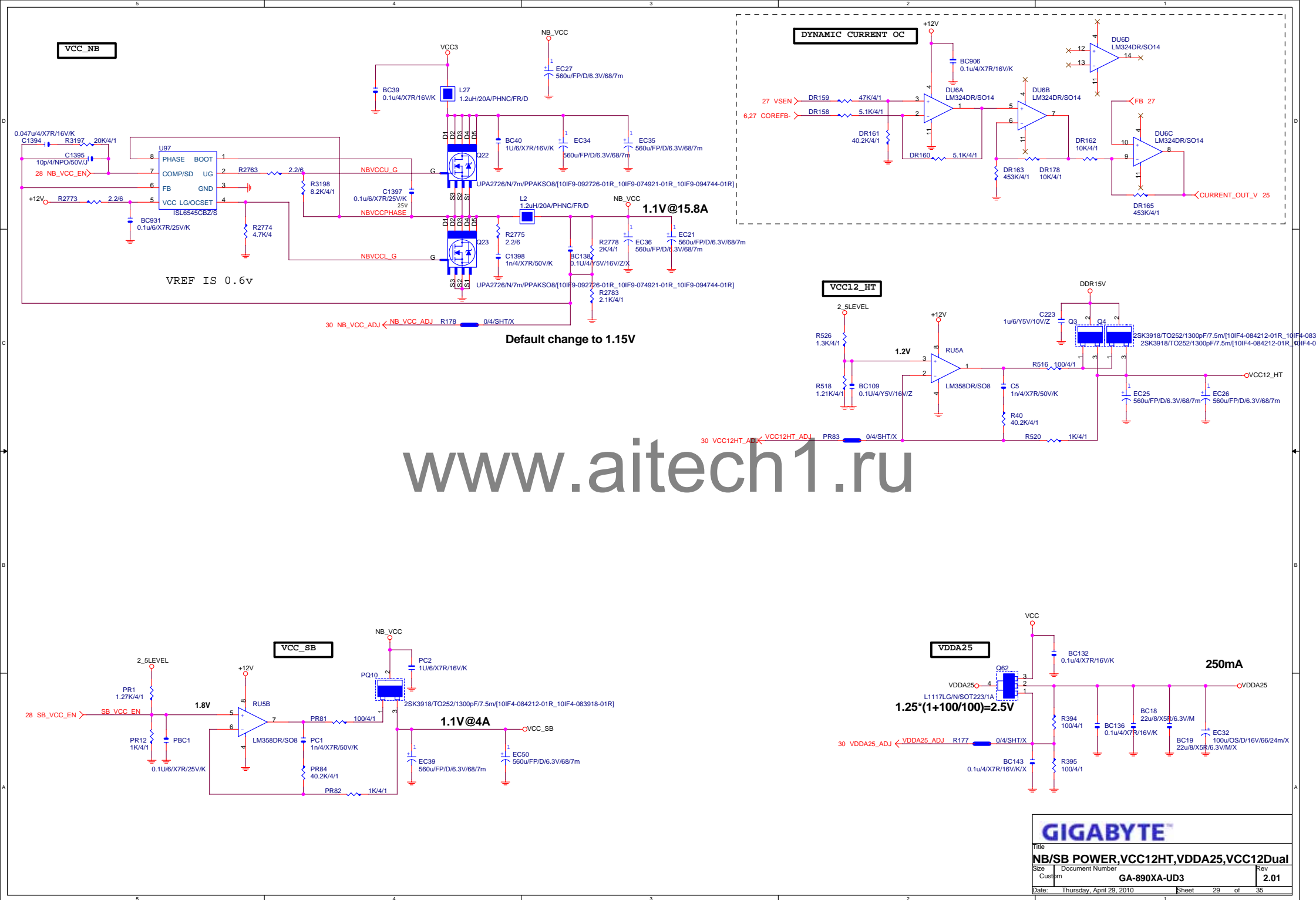
**GIGABYTE™**

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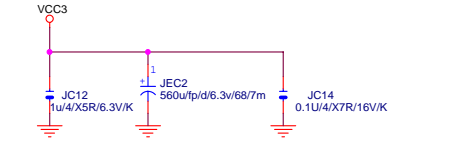
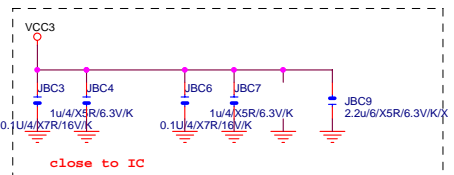
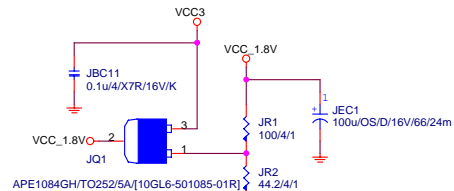
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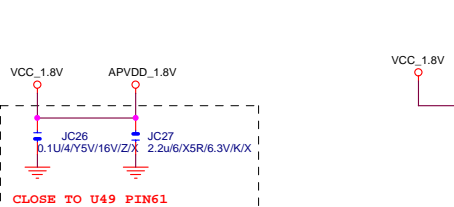
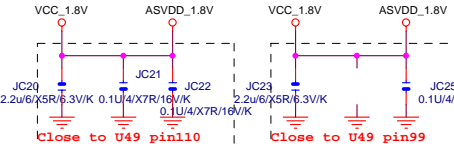
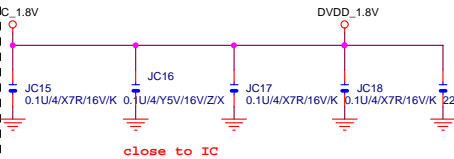
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**NB/SB POWER,VCC12HT,VDDA25,VCC12Dual**  
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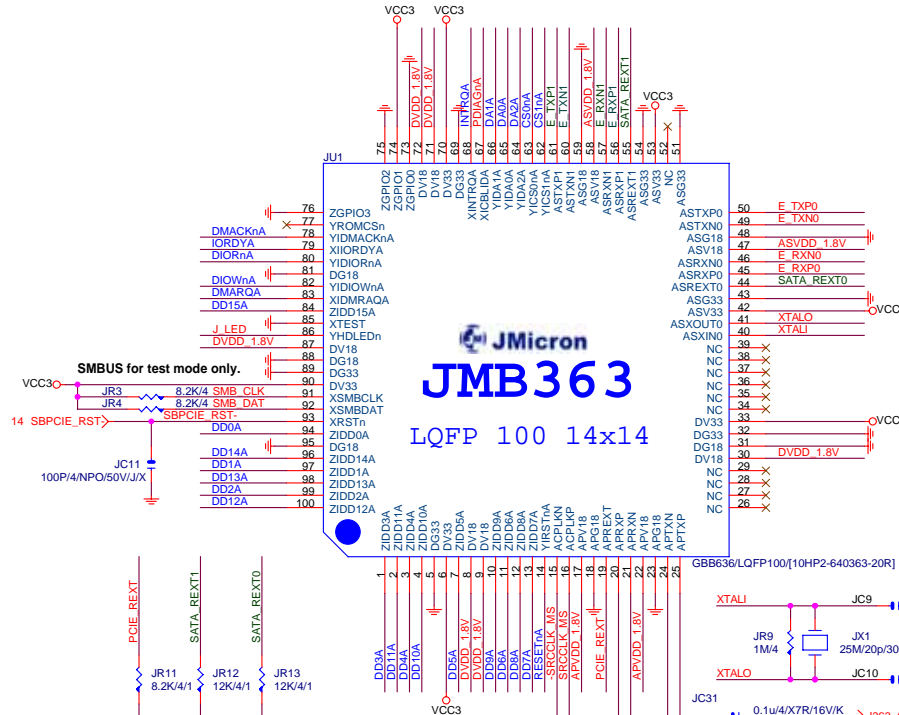
### 3.3V to 1.8V Voltage Regulator



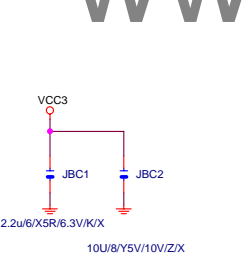
close to U49 pin94 and pin105



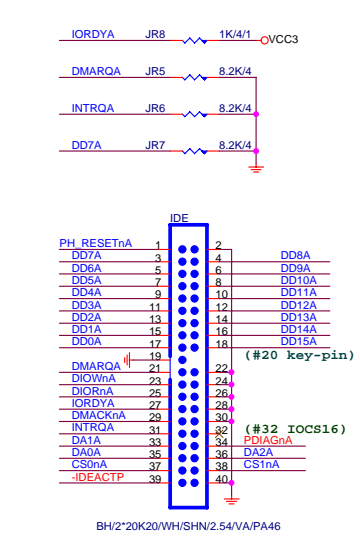
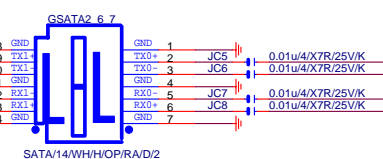
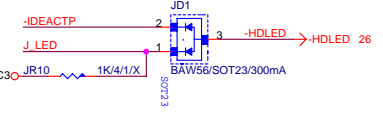
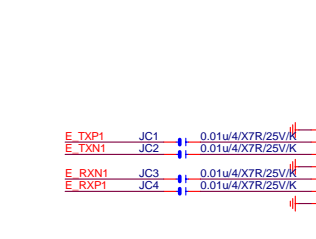
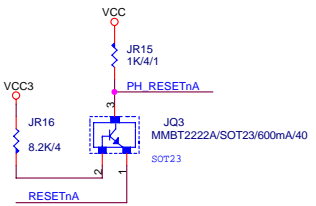
CLOSE TO U49 PIN61



Near to PIN Check SATA eye PCIE\_RST -> 8.06K/4/1

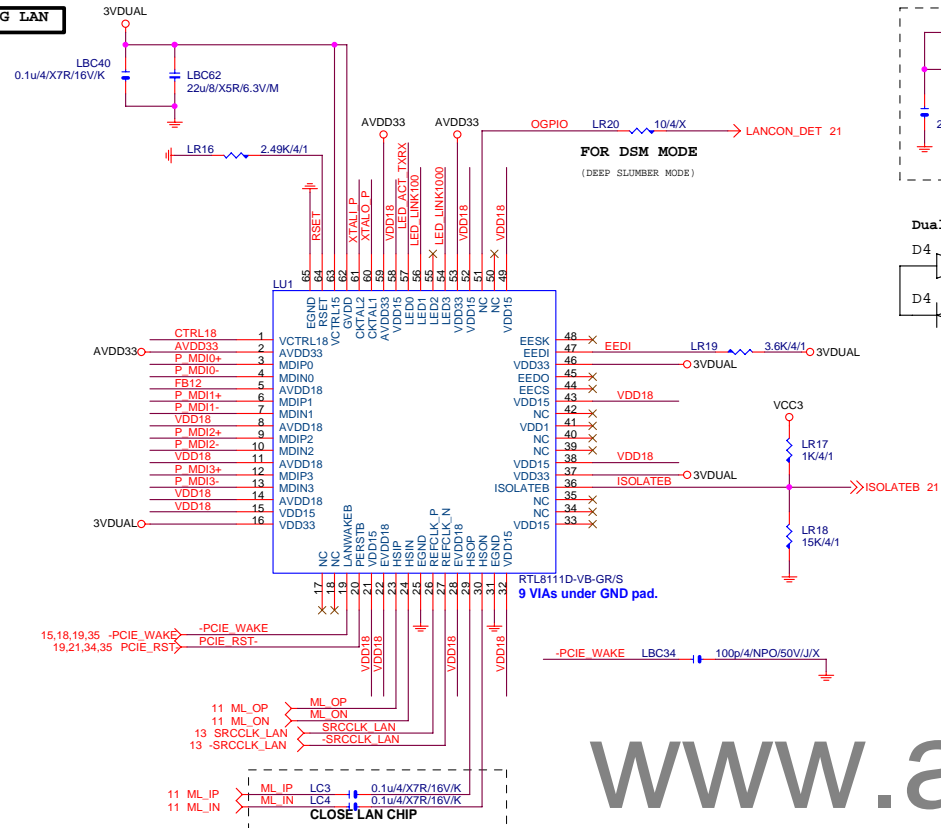


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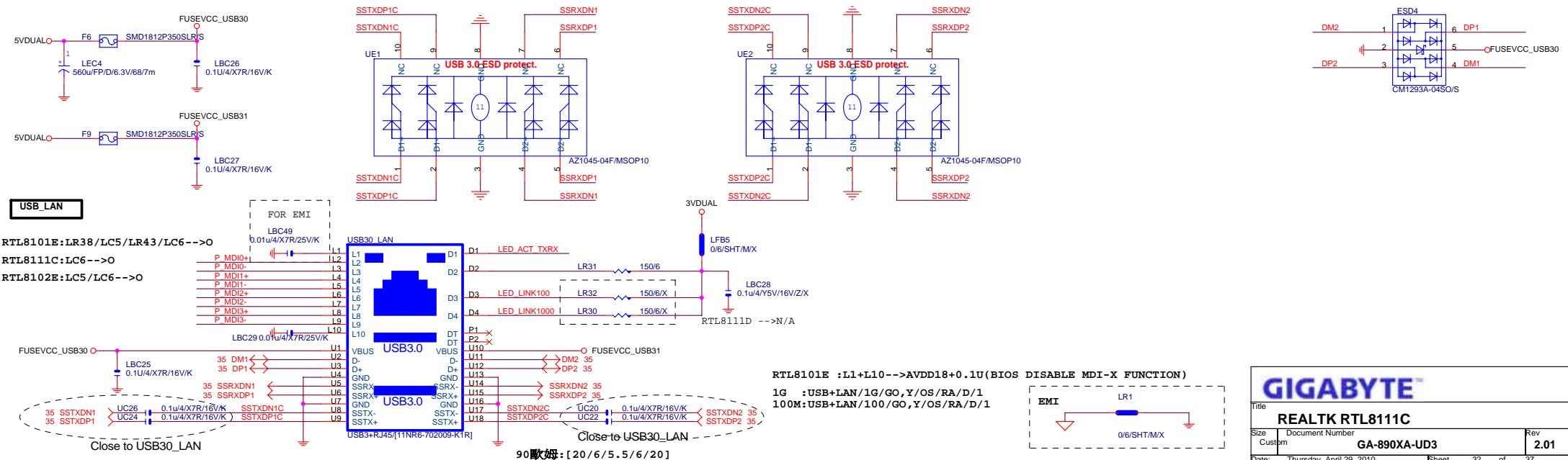


# PCIE-1G LAN



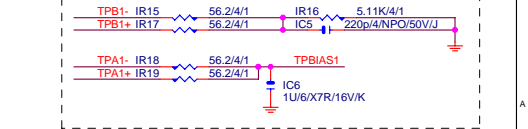
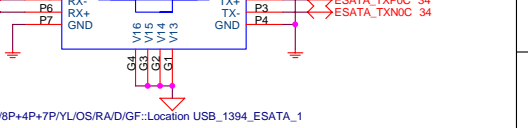
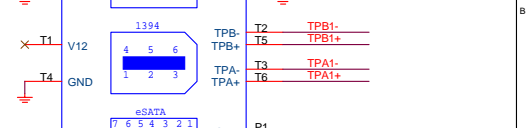
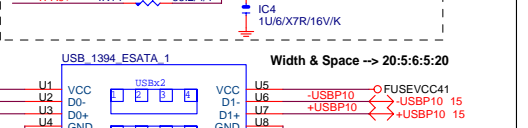
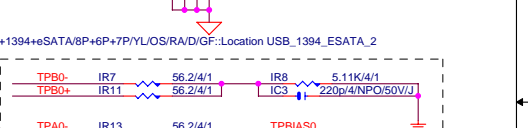
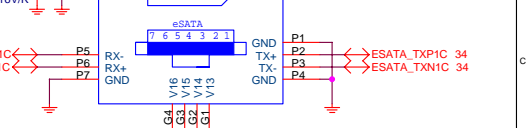
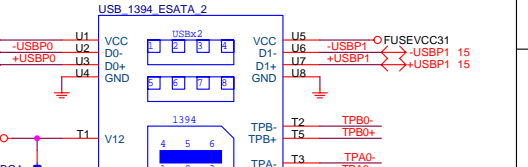
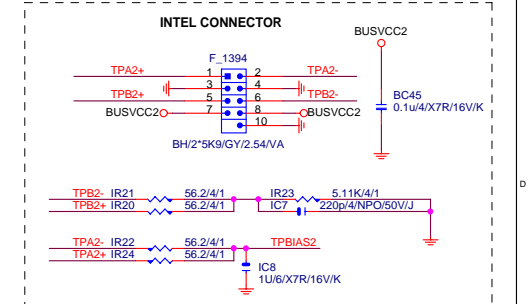
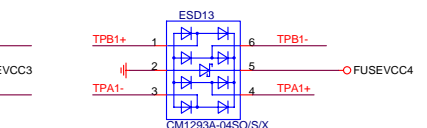
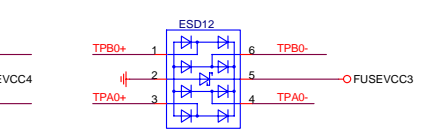
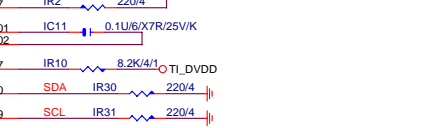
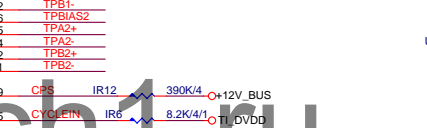
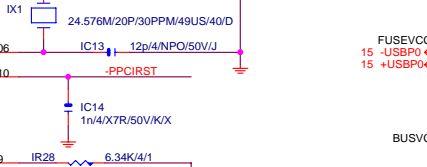
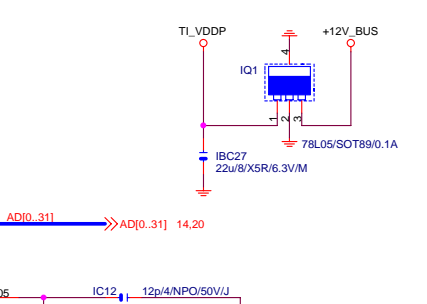
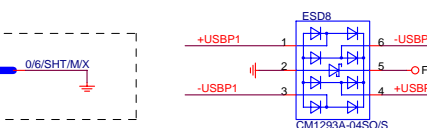
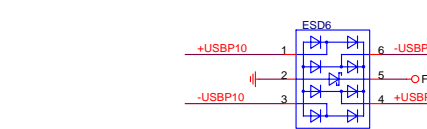
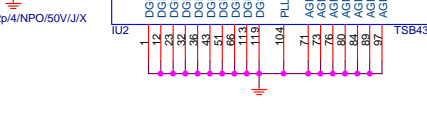
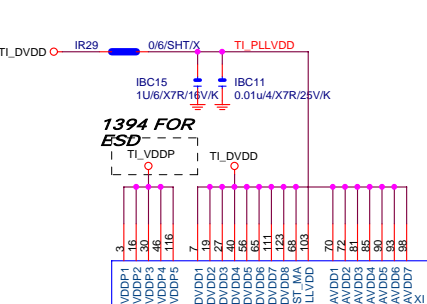
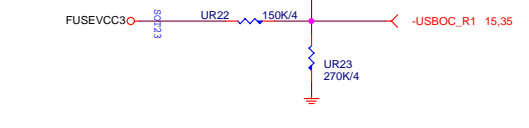
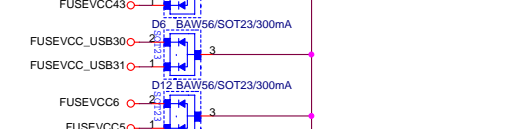
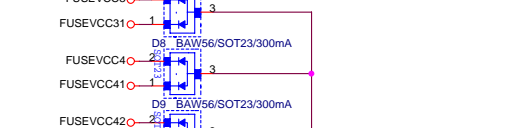
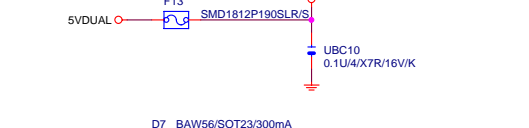
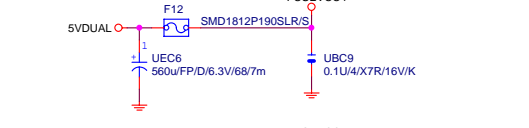
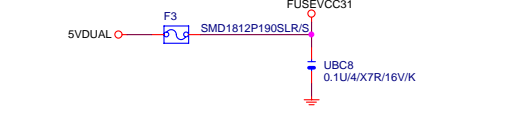
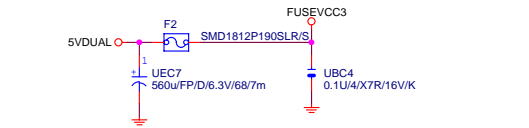
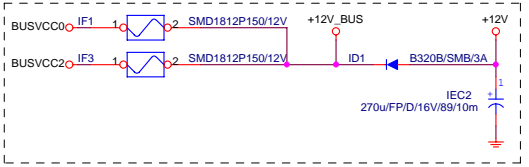
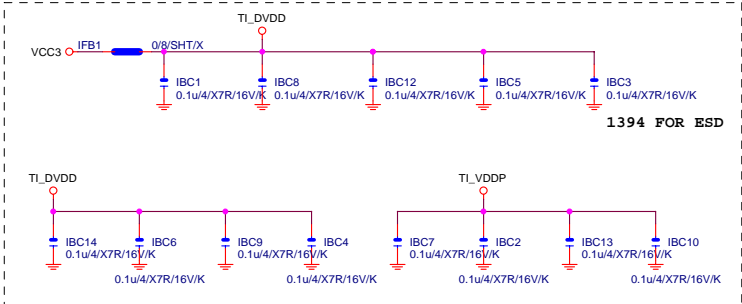
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# USB\_LAN



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